SAMA5D27 Wireless SOM1

ATSAMA5D27-WLSOM1

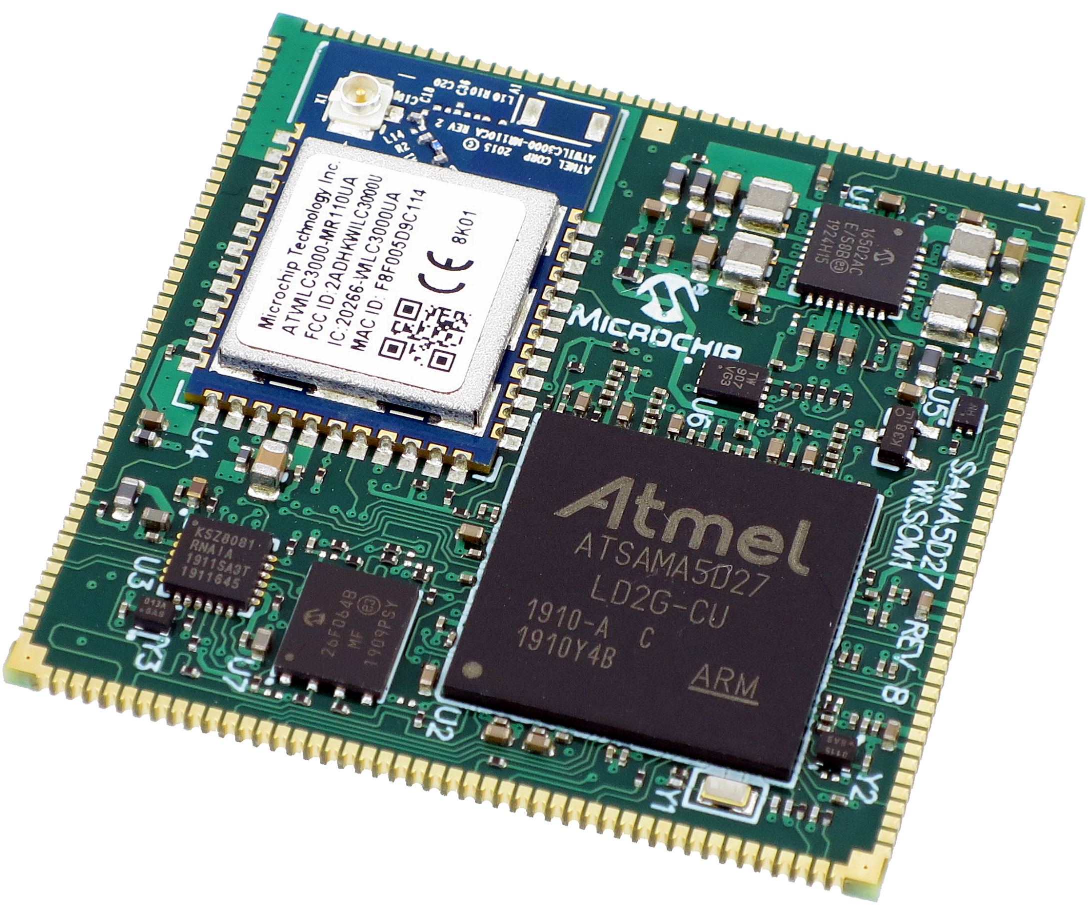
Introduction

The Microchip SAMA5D27 Wireless System-On-Module 1 (ATSAMA5D27-WLSOM1) is a small single-sided SOM based on the high-performance System-in-Package (SiP) 32-bit Arm® Cortex®-A5 processor-based MPU SAMA5D27, 2 Gb LPDDR2 SDRAM running up to 500 MHz, and Wi-Fi® plus Bluetooth® (Wi-Fi/BT) Wireless module.

The ATSAMA5D27-WLSOM1 is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The ATSAMA5D27-WLSOM1 also limits design rules of the main application board, reducing overall PCB complexity and cost. The ATSAMA5D27-WLSOM1 is delivered with a free Linux® distribution and bare metal C examples.

Figure 1. ATSAMA5D27-WLSOM1 Overview



Features

- System-In-Package (ATSAMA5D27C-LD2G-CU) Including:
  - Arm® Cortex®-A5 processor-based SAMA5D27 MPU
  - 2 Gbit LPDDR2 SDRAM
- On-Board Power Management Unit (MCP16502AC-E/S8B)
- 64 Mb Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- IEEE® 802.11 b/g/n Wi-Fi plus Bluetooth (Wi-Fi/BT) Module (ATWILC3000-MR110UA)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA)
- ATECC608A Secure Element
- MEMS Oscillators for Clock Generation
- 40.8 x 40.8 mm Module, Pitch 0.8mm, Solderable Manually for Prototyping
- 94 I/Os
- Up to 7 Tamper Pins
- One USB Device, one USB Host and one HSIC Interface
- Shutdown and Reset Control Pins
- Independent Power Supplies Available for Camera Sensor, for SD Card and for Backup Depending on Voltage Domains
- Operational Specifications:
  - Main operating voltage: 3.0V to 5.5V ± 5%
  - Temperature range: -40°C to 85°C
  - Integrated oscillators, internal voltage regulators
  - Multiple interfaces and I/Os for easy application development

Applications

- Industrial Control and Automation
- Smart Appliances
- Human Machine Interfaces (HMI)
- IoT Gateway
- Access Control Panels
- Security and Alarm Systems

Table of Contents

1. Reference Documents

The following reference data sheets are available on www.microchip.com:

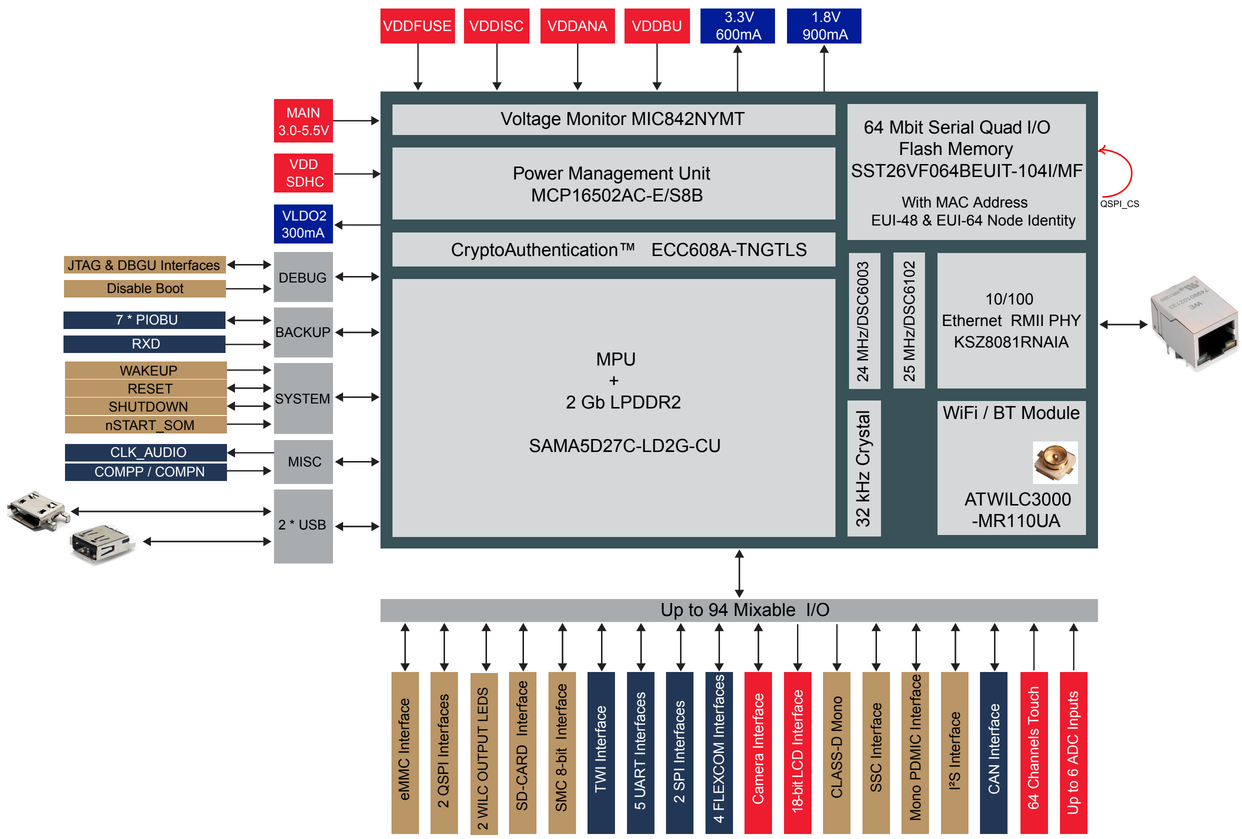
Table 1-1. Reference Data Sheets

Document Title	Available
KSZ8081RNA/RND	https://www.microchip.com/wwwproducts/en/KSZ8081
SAMA5D2 SIP	https://www.microchip.com/wwwproducts/en/ATSAMA5D27C-LD2G
SST26VF064BEUI	https://www.microchip.com/wwwproducts/en/SST26VF064BEUI
MCP16502	https://www.microchip.com/wwwproducts/en/MCP16502
MIC841/2	https://www.microchip.com/wwwproducts/en/MIC842
DSC60XXB	https://www.microchip.com/wwwproducts/en/DSC6000B
DSC61XXB	https://www.microchip.com/wwwproducts/en/DSC6100B
ATWILC3000-MR110UA	https://www.microchip.com/wwwproducts/en/ATWILC3000
ATECC608A	https://www.microchip.com/wwwproducts/en/ATECC608A

2. Block Diagram

The following figure shows the block diagram of the ATSAMA5D27-WLSOM1 module.

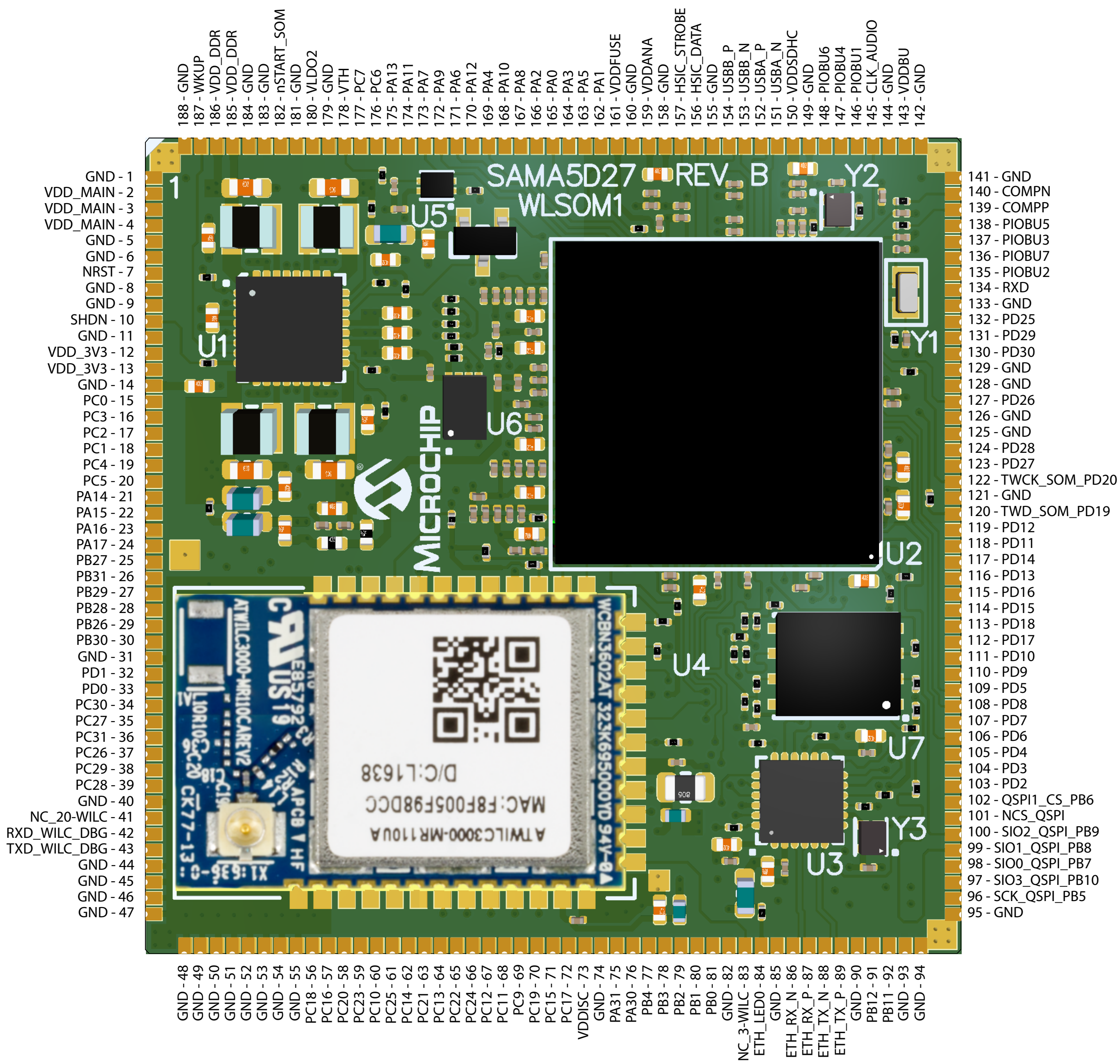
Figure 2-1. ATSAMA5D27-WLSOM1 Module Block Diagram



3. Pinout

3.1 Pinout Overview

Figure 3-1. ATSAMA5D27-WLSOM1 Pin Assignment



3.2 Pin List

The following tables provide the SAMA5D27-WLSOM1 module pin description.

Table 3-1. Pin Description: PIOA

Pin #	Pin Name	Power Rail	Description
165	PA0	VDDSDHC	Configurable GPIO PA0
162	PA1	VDDSDHC	Configurable GPIO PA1
166	PA2	VDDSDHC	Configurable GPIO PA2
164	PA3	VDDSDHC	Configurable GPIO PA3
169	PA4	VDDSDHC	Configurable GPIO PA4
163	PA5	VDDSDHC	Configurable GPIO PA5
171	PA6	VDDSDHC	Configurable GPIO PA6
173	PA7	VDDSDHC	Configurable GPIO PA7
167	PA8	VDDSDHC	Configurable GPIO PA8
172	PA9	VDDSDHC	Configurable GPIO PA9
168	PA10	VDDSDHC	Configurable GPIO PA10
174	PA11	VDD_3V3	Configurable GPIO PA11
170	PA12	VDD_3V3	Configurable GPIO PA12
175	PA13	VDD_3V3	Configurable GPIO PA13
21	PA14	VDD_3V3	Configurable GPIO PA14
22	PA15	VDD_3V3	Configurable GPIO PA15
23	PA16	VDD_3V3	Configurable GPIO PA16
24	PA17	VDD_3V3	Configurable GPIO PA17
76	PA30	VDD_3V3	Configurable GPIO PA30
75	PA31	VDD_3V3	Configurable GPIO PA31

Table 3-2. Pin Description: PIOB

Pin #	Pin Name	Power Rail	Description
81	PB0	VDD_3V3	Configurable GPIO PB0
80	PB1	VDD_3V3	Configurable GPIO PB1
79	PB2	VDD_3V3	Configurable GPIO PB2
78	PB3	VDD_3V3	Configurable GPIO PB3
77	PB4	VDD_3V3	Configurable GPIO PB4
96	SCK_QSPI_PB5	VDD_3V3	QSPI Serial Clock
102	QSPI1_CS_PB6	VDD_3V3	QSPI Chip Select Output Control
98	SIO0_QSPI_PB7	VDD_3V3	QSPI Serial Data Input/Output 0
99	SIO1_QSPI_PB8	VDD_3V3	QSPI Serial Data Input/Output 1
100	SIO2_QSPI_PB9	VDD_3V3	QSPI Serial Data Input/Output 2
97	SIO3_QSPI_PB10	VDD_3V3	QSPI Serial Data Input/Output 3
92	PB11	VDD_3V3	Configurable GPIO PB11

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Pin #	Pin Name	Power Rail	Description
91	PB12	VDD_3V3	Configurable GPIO PB12
29	PB26	VDD_3V3	Configurable GPIO PB26
25	PB27	VDD_3V3	Configurable GPIO PB27
28	PB28	VDD_3V3	Configurable GPIO PB28
27	PB29	VDD_3V3	Configurable GPIO PB29
30	PB30	VDD_3V3	Configurable GPIO PB30
26	PB31	VDD_3V3	Configurable GPIO PB31

Table 3-3. Pin Description: PIOC

Pin #	Pin Name	Power Rail	Description
15	PC0	VDD_3V3	Configurable GPIO PC0
18	PC1	VDD_3V3	Configurable GPIO PC1
17	PC2	VDD_3V3	Configurable GPIO PC2
16	PC3	VDD_3V3	Configurable GPIO PC3
19	PC4	VDD_3V3	Configurable GPIO PC4
20	PC5	VDD_3V3	Configurable GPIO PC5
176	PC6	VDD_3V3	Configurable GPIO PC6
177	PC7	VDD_3V3	Configurable GPIO PC7
69	PC9	VDDISC	Configurable GPIO PC9
60	PC10	VDDISC	Configurable GPIO PC10
68	PC11	VDDISC	Configurable GPIO PC11
67	PC12	VDDISC	Configurable GPIO PC12
64	PC13	VDDISC	Configurable GPIO PC13
62	PC14	VDDISC	Configurable GPIO PC14
71	PC15	VDDISC	Configurable GPIO PC15
57	PC16	VDDISC	Configurable GPIO PC16
72	PC17	VDDISC	Configurable GPIO PC17
56	PC18	VDDISC	Configurable GPIO PC18
70	PC19	VDDISC	Configurable GPIO PC19
58	PC20	VDDISC	Configurable GPIO PC20
63	PC21	VDDISC	Configurable GPIO PC21
65	PC22	VDDISC	Configurable GPIO PC22
59	PC23	VDDISC	Configurable GPIO PC23
66	PC24	VDDISC	Configurable GPIO PC24
61	PC25	VDDISC	Configurable GPIO PC25

...........continued

Pin #	Pin Name	Power Rail	Description
37	PC26	VDD_3V3	Configurable GPIO PC26
35	PC27	VDD_3V3	Configurable GPIO PC27
39	PC28	VDD_3V3	Configurable GPIO PC28
38	PC29	VDD_3V3	Configurable GPIO PC29
34	PC30	VDD_3V3	Configurable GPIO PC30
36	PC31	VDD_3V3	Configurable GPIO PC31

Table 3-4. Pin Description: PIOD

Pin #	Pin Name	Power Rail	Description
33	PD0	VDD_3V3	Configurable GPIO PD0
32	PD1	VDD_3V3	Configurable GPIO PD1
103	PD2	VDD_3V3	Configurable GPIO PD2
104	PD3	VDDANA	Configurable GPIO PD3
105	PD4	VDDANA	Configurable GPIO PD4
109	PD5	VDDANA	Configurable GPIO PD5
106	PD6	VDDANA	Configurable GPIO PD6
107	PD7	VDDANA	Configurable GPIO PD7
108	PD8	VDDANA	Configurable GPIO PD8
110	PD9	VDDANA	Configurable GPIO PD9
111	PD10	VDDANA	Configurable GPIO PD10
118	PD11	VDDANA	Configurable GPIO PD11
119	PD12	VDDANA	Configurable GPIO PD12
116	PD13	VDDANA	Configurable GPIO PD13
117	PD14	VDDANA	Configurable GPIO PD14
114	PD15	VDDANA	Configurable GPIO PD15
115	PD16	VDDANA	Configurable GPIO PD16
112	PD17	VDDANA	Configurable GPIO PD17
113	PD18	VDDANA	Configurable GPIO PD18
120	TWD_SOM_PD19	VDDANA	I²C Data Line
122	TWCK_SOM_PD20	VDDANA	I²C Clock Line
132	PD25	VDDANA	Configurable GPIO PD25
127	PD26	VDDANA	Configurable GPIO PD26
123	PD27	VDDANA	Configurable GPIO PD27
124	PD28	VDDANA	Configurable GPIO PD28
131	PD29	VDDANA	Configurable GPIO PD29

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Pin #	Pin Name	Power Rail	Description
130	PD30	VDDANA	Configurable GPIO PD30

Table 3-5. Pin Description: System

Pin #	Pin Name	Power Rail	Description
145	CLK_AUDIO	VDD_3V3	Audio Master Clock Frequency Output
151	USBA_N	VDD_3V3	USB Host Port A High-Speed Data -
152	USBA_P	VDD_3V3	USB Host Port A High-Speed Data +
157	HSIC_STROBE	VDDHSIC (1.2V)	USB High-Speed Inter-Chip Strobe
156	HSIC_DATA	VDDHSIC (1.2V)	USB High-Speed Inter-Chip Data
153	USBB_N	VDD_3V3	USB Host Port B High-Speed Data -
154	USBB_P	VDD_3V3	USB Host Port B High-Speed Data +
7	NRST	VDDBU	Module Reset
140	COMPN	VDDBU	External Analog Data Input
139	COMPP	VDDBU	External Analog Data Input
146	PIOBU1	VDDBU	Tamper I/O #1
135	PIOBU2	VDDBU	Tamper I/O #2
137	PIOBU3	VDDBU	Tamper I/O #3
147	PIOBU4	VDDBU	Tamper I/O #4
138	PIOBU5	VDDBU	Tamper I/O #5
148	PIOBU6	VDDBU	Tamper I/O #6
136	PIOBU7	VDDBU	Tamper I/O #7
134	RXD	VDDBU	RXLP Receive Data Input
10	SHDN	VDDBU	Shutdown Control
187	WKUP	VDDBU	Module Wake-Up
178	VTH	VDD_MAIN	Low Voltage Threshold Detection Input
101	NCS_QSPI	VDD_3V3	Embedded QSPI Chip Select Input
83	NC	–	Not connected
41	NC	–	Not connected
89	ETH_TX_P	–	Physical Transmit Signal (+ differential)
88	ETH_TX_N	–	Physical Transmit Signal (– differential)
87	ETH_RX_P	–	Physical Receive Signal (+ differential)
86	ETH_RX_N	–	Physical Receive Signal (– differential)
84	ETH_LED0	VDD_3V3	Programmable LED0 Output
182	nSTART_SOM	VDD_MAIN	Module Start-up Control Input
42	RXD_WILC_DBG	VDD_3V3	Used for Radio Debug. UART RXD

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Pin #	Pin Name	Power Rail	Description
43	TXD_WILC_DBG	VDD_3V3	Used for Radio Debug. UART TXD

Table 3-6. Pin Description: Power

Pin #	Pin Name	Power Rail	Type	Description
1, 5, 6, 8, 9, 11, 14, 31, 40, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 74, 82, 85, 90, 93, 94, 95, 121, 125, 126, 129, 133, 141, 142, 144, 128, 149, 155, 158, 160, 179, 181, 183, 184, 188	GND	GND	GND	Ground
159	VDDANA	VDDANA	I	Analog Voltage Input
143	VDDBU	VDDBU	I	Backup Voltage Input
161	VDDFUSE	VDDFUSE	I	VDDFUSE Voltage Input
73	VDDISC	VDDISC	I	VDDISC Voltage Input
2, 3, 4	VDD_MAIN	VDD_MAIN	I	Main input Voltage
12, 13	VDD_3V3	VDD_3V3	O	3.3V Voltage Output
180	VLDO2	VLDO2	O	VLDO2 Output Voltage
150	VDDSDHC	VDDSDHC	I	VDDSDHC Input Voltage
185, 186	VDD_DDR	VDD_DDR	O	1.8V Output Voltage

4. Functional Description

4.1 MPU and Memory Subsystem

4.1.1 SAMA5D27 System-In-Package

The SAMA5D27 System-In-Package (SiP) (ATSAMA5D27C-LD2G-CU) integrates the ARM Cortex-A5 processor-based SAMA5D2 MPU with 2 Gbit LPDDR2-SDRAM in a single package.

By combining the high-performance, ultra-low power SAMA5D2 with LPDDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced. This makes board design easier and lowers the overall cost of the bill of materials. Board design is more robust by facilitating design for EMI, ESD and signal integrity.

For more information about the SiP, refer to 1. Reference Documents. This section lists the sole reference documents for product information on the SAMA5D2 and the LPDDR2-SDRAM memory.

The ATSAMA5D27C-LD2G-CU is available in a 361-ball TFBGA package.

Connections of the supplies and the system pins of the ATSAMA5D27C-LD2G-CU are described in the following schematics.

Figure 4-1. SAMA5D27 SiP Schematic

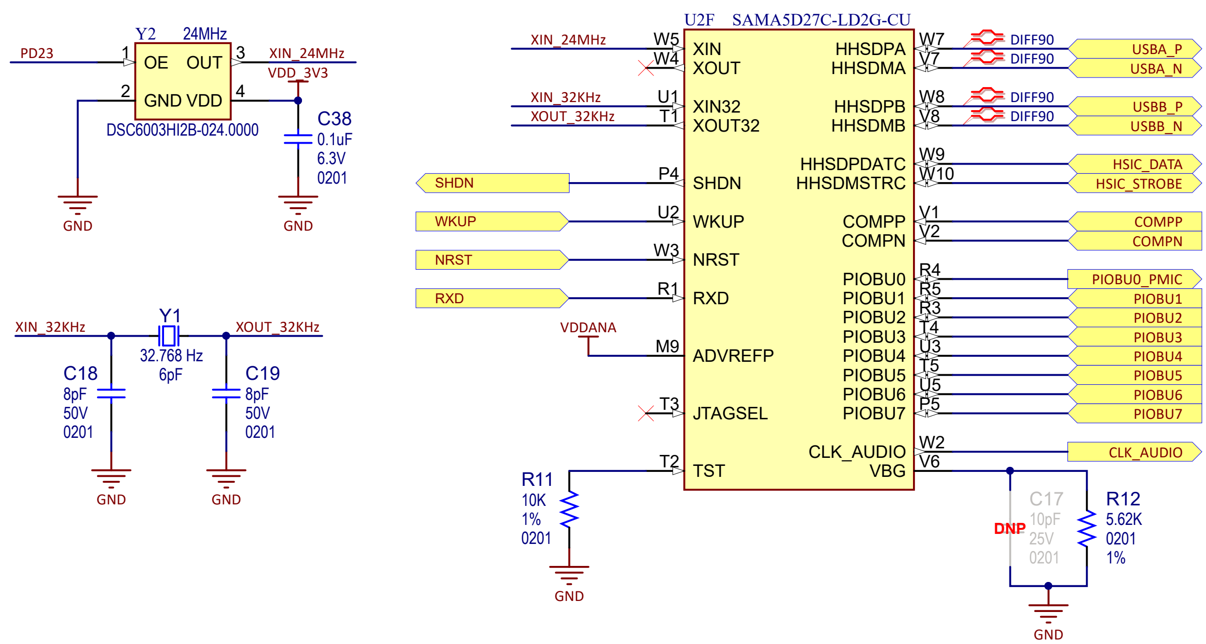
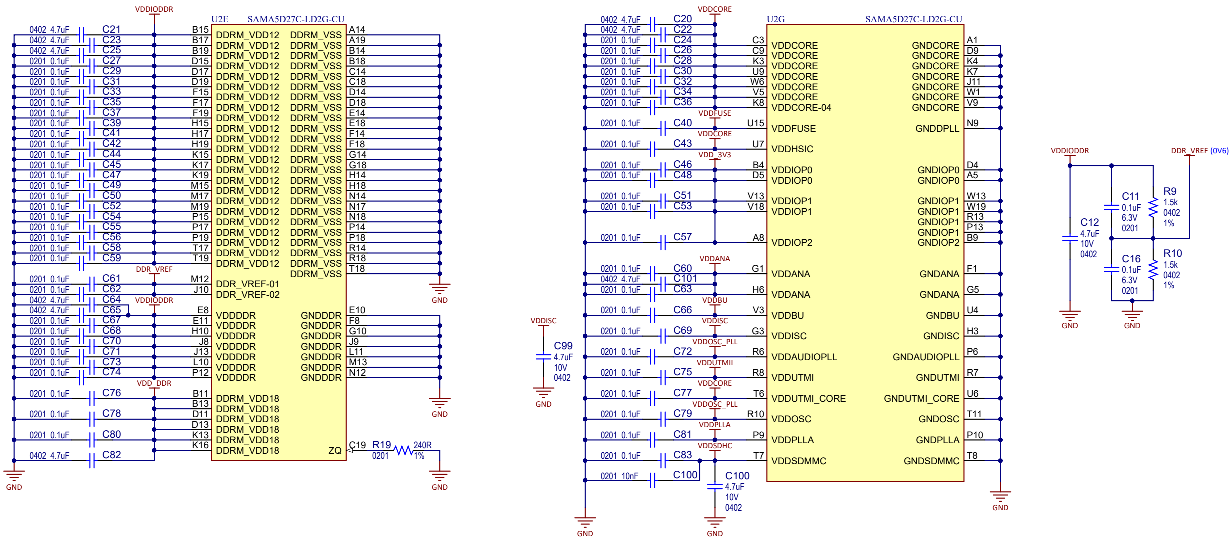


Figure 4-2. SAMA5D27 SiP Decoupling Schematic



4.1.2 Power Management Unit

The MCP16502 is a full-featured PMIC optimized for Microchip MPU devices.

The MCP16502 integrates four DC-DC buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an Interrupt flag and an I^{2}C interface.

All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.

Two 300mA LDOs are provided such that sensitive analog loads can be supported.

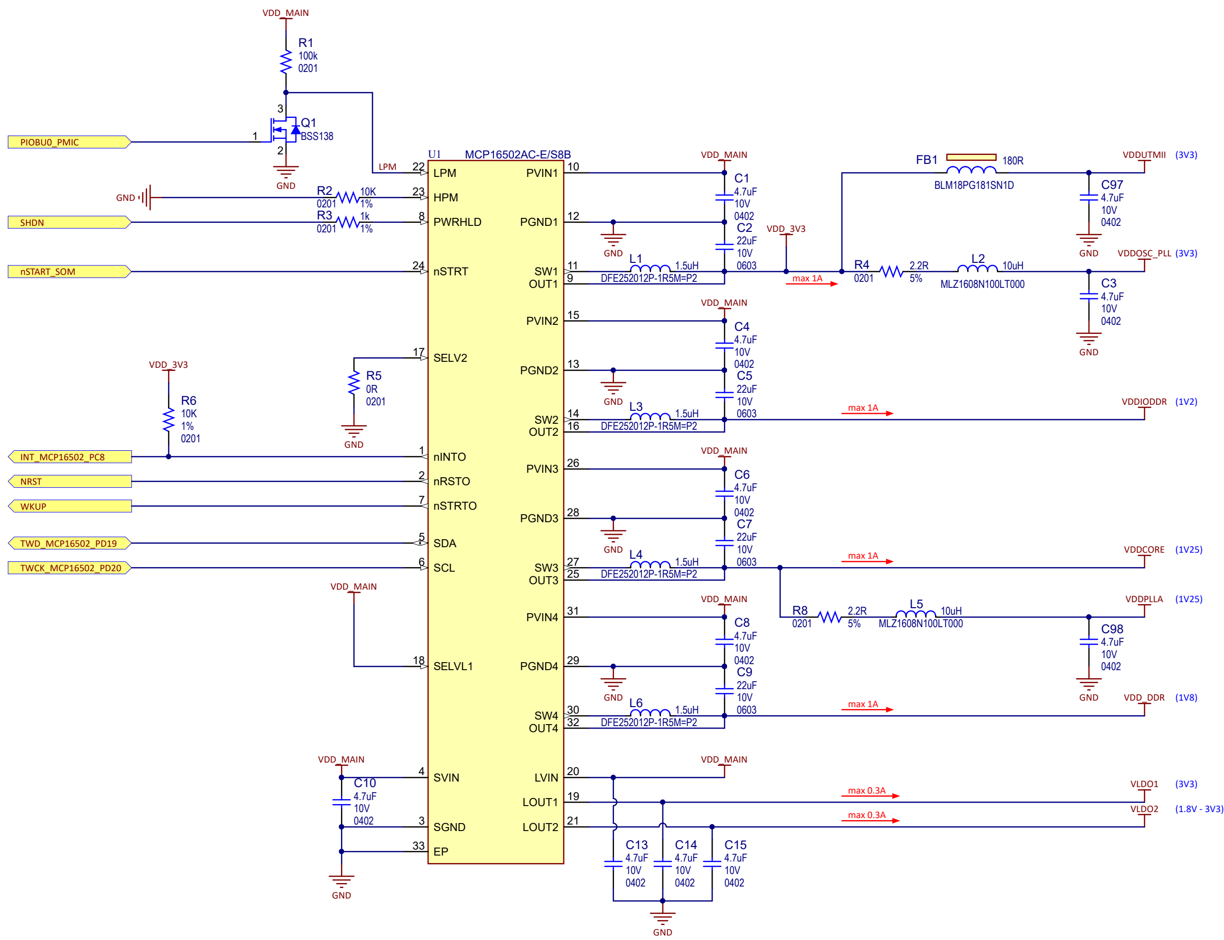
The default power channel sequencing is built-in, according to the requirements of the Microchip MPU device.

The MCP16502 features a low no-load operational quiescent current, and it draws less than 10 uA in full shutdown.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package with an operating junction temperature range from –40°C to +125°C. It is AEC-Q100 Grade 2 (T_{AMB}=105°C) qualified.

Figure 4-3. Power Management Unit Schematic



4.1.3 SQI Memory

4.1.3.1 Description and Schematic

The ATSAMA5D27-WLSOM1 embeds the SST26VF064BEUIT-104I/MF, a 64 Mb Serial Quad I/O Flash memory.

The SST26VF064BEUIT-104I/MF SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

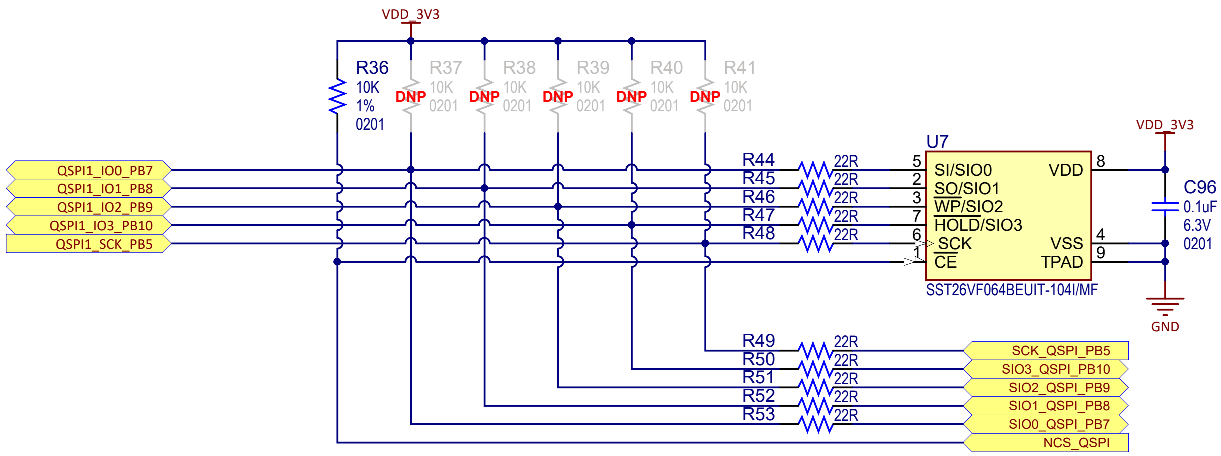
The SST26VF064BEUIT-104I/MF also embeds EUI-48 and EUI-64 MAC addresses.

The SST26VF064BEUIT-104I/MF is available in 8-lead WDFN package with 6 mm × 5 mm dimensions.

For more information, refer to the product web page.

It is possible to deselect the Chip Enable of the embedded QSPI to use external one. In this case, the NCS_QSPI pin must be left floating and the signal QSPI1_CS_PB6 must be connected to an external QSPI Chip Select.

Figure 4-4. QSPI Memory Schematic



4.1.3.2 MAC Address

The SST26VF064BEUI is pre-programmed at the factory with globally unique EUI-48 and EUI-64 node identifiers. The addresses are located in the Serial Flash Discoverable Parameters (SFDP) table and accessible via the SFDP read instruction.

The 6-byte EUI-48 address value of the SST26VF064BEUI is stored in the SFDP table at address locations 0x261 through 0x266.

The 8-byte EUI-64 address value of the SST26VF064BEUI is stored in the SFDP table at address locations 0x268 through 0x26F.

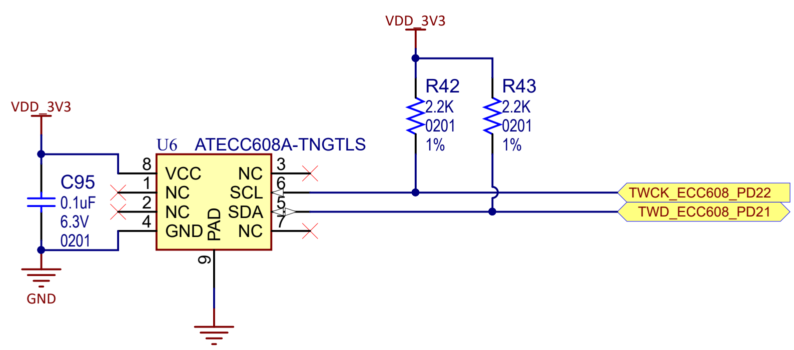
For more information, refer to the product web page.

4.1.4 Secure Element

The ATECC608A is a member of the Microchip CryptoAuthentication™ family of high-security cryptographic devices which combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

The ATECC608A has a flexible command set that allows use in many applications, including Network/IoT Node Endpoint Security, Secure Boot, Small Message Encryption, Key Generation for Software Download and Ecosystem control and Anti-Counterfeiting.

Figure 4-5. ECC608A Secure Element Schematic



4.2 Power Management

4.2.1 Power Architecture

Basic operation of the ATSAMA5D27-WLSOM1 requires a +5.0V input voltage supply, and a VDDBU (+1.65V to +3.6V) input voltage supply generally ensured by a backup battery. +5.0V power is supplied to the VDD_MAIN domain.

⚠ CAUTION As a general design rule, it is recommended to connect all input supply pins, except VDDFUSE which must be connected to GND by a 100 Ohms resistor if not used, to your power supply and at least a matching number of ground (GND) pins. For the best EMI performance, it is recommended to connect ALL ground pins of the ATSAMA5D27-WLSOM1 module to a solid ground plane.

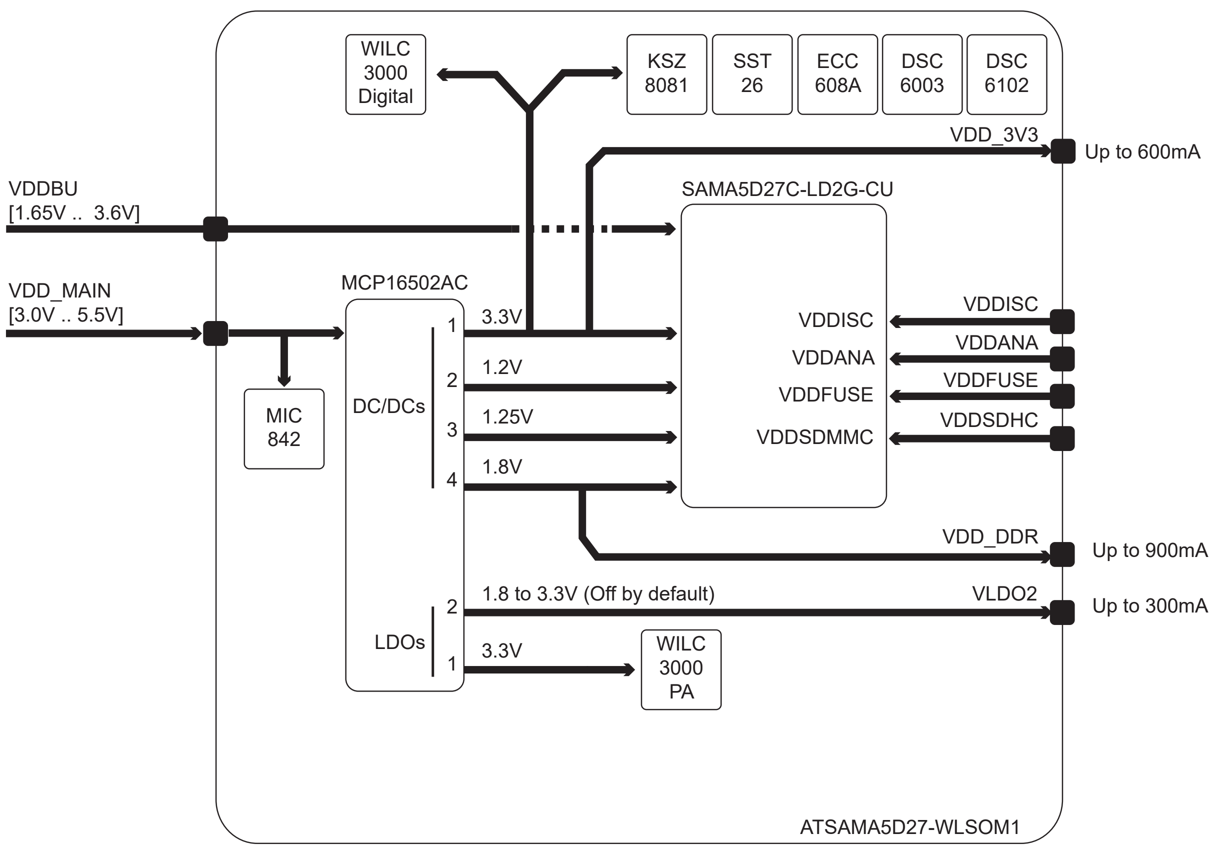
Power-on is controlled through the nSTART_SOM signal. This signal must be provided by the host board, e.g. via an automated reset controller or a push-button.

The ATSAMA5D27-WLSOM1 module can operate from a single voltage supply (VDD_MAIN) with a value comprised between +3.0V and +5.5V and, with the MCP16502 PMIC device, internally generates the voltage supplies required by the SAMA5D2 processor and on-board components.

The PMIC on-board switching regulators generates the 3.3V, 1.20V, 1.25V and 1.8V voltage supplies required by the SAMA5D27 processor and onboard components.

The ATSAMA5D27-WLSOM1 delivers external power supplies to main board application such as VDD_DDR (1.8V with 900 mA current capability), VDD_3V3 (3.3V with 600mA output current capability) and VLDO2 output (1.8V to 3.3V with 300 mA output current capability).

Figure 4-6. ATSAMA5D27-WLSOM1 Power Architecture



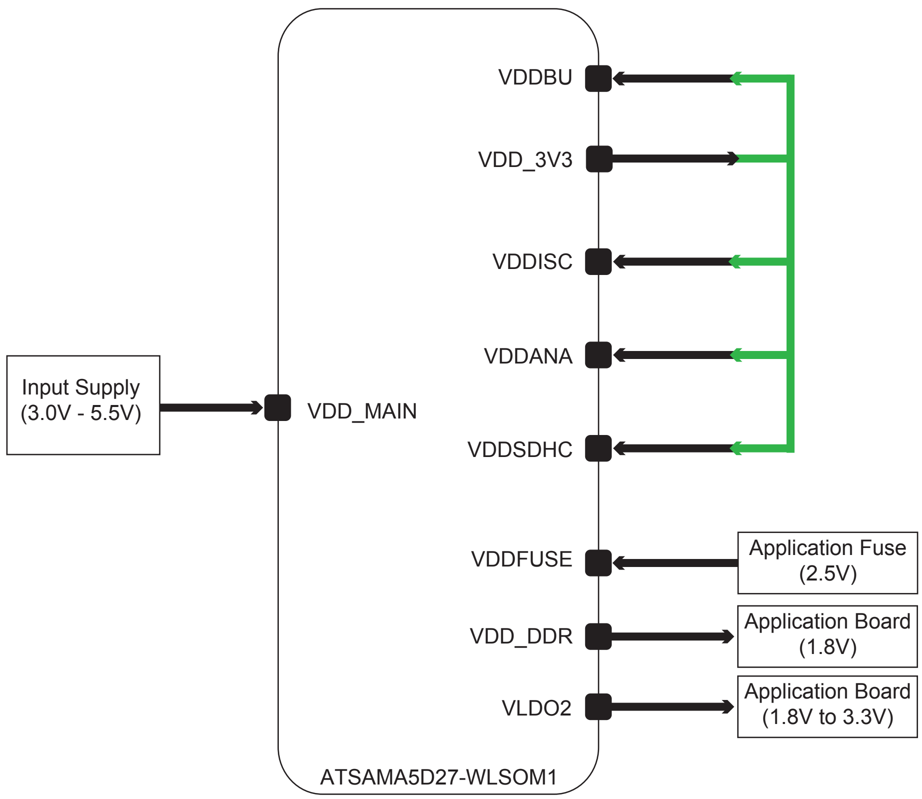
4.2.2 Various Power Configurations

Two different configurations are described below, depending on customer use.

- Single Supply—ATSAMA5D27-WLSOM1 can be supplied by only one input supply (e.g. 5V AC/DC wall adapter) and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All the PIO lines are supplied at 3.3V.
- Multiple Supplies—ATSAMA5D27-WLSOM1 can be supplied by 5V and by a backup battery. Some PIO lines are supplied by different LDOs for specific applications, such as an ISC camera or a high-speed SD card.

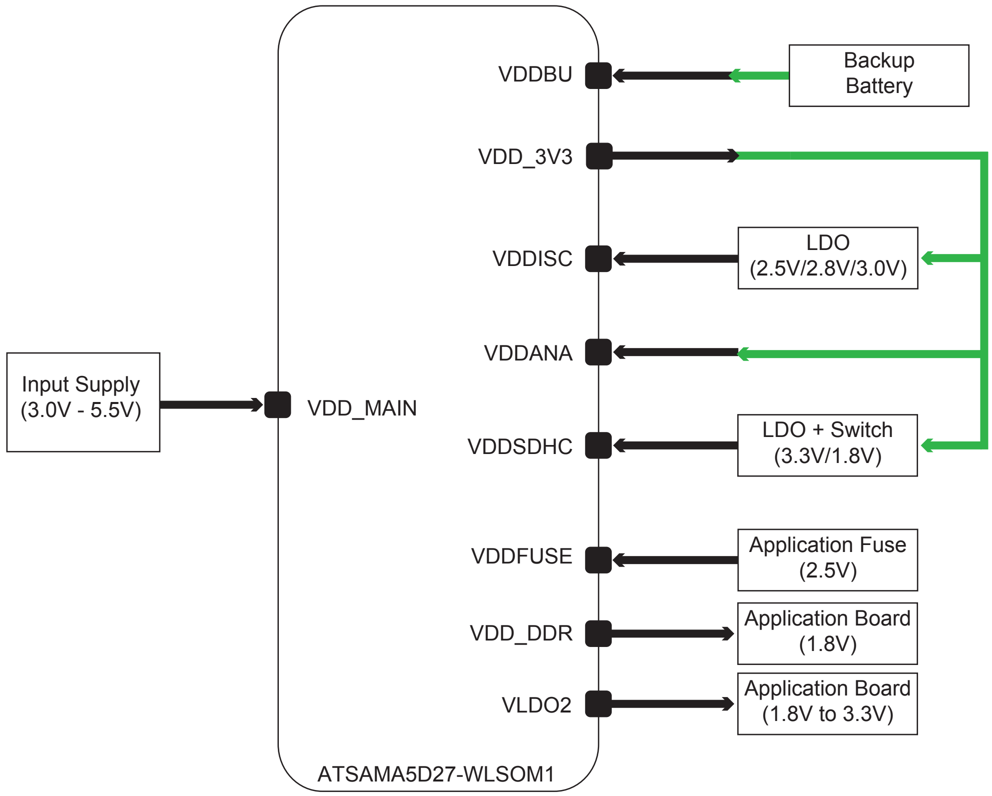
4.2.2.1 Power Configurations: Single Supply

Figure 4-7. ATSAMA5D27-WLSOM1 Single Supply Connection Example



4.2.2.2 Power Configurations: Multiple Supplies

Figure 4-8. ATSAMA5D27-WLSOM1 Multiple Supplies Connection Example



4.2.3 Power On/Off Sequences

4.2.3.1 LPDDR2 Power-Off Sequence

The LPDDR2 power-off sequence must be controlled by software to preserve the LPDDR2 device.

In this sequence, the CKE signal should be low during the full period the power rails are powering down.

The power failure can be controlled by the embedded Voltage Supervisor (MIC842) and handled at system level (IRQ on PD31). The LPDDR2 power-off sequence is applied using the bit LPDDR2_LPDDR3_PWOFF in the MPDDRC Low-Power register (MPDDRC_LPR).

For more information, refer to the following documents:

- SAMA5D2 Series Data sheet available on https://www.microchip.com/, sections *LPDDR2 Power Fail Management* and *MPDDRC Low-Power Register*
- Jedec Standard *Low Power Double Data Rate 2 (LPDDR2)*, JESD209-2B

Note: An uncontrolled power-off sequence can be applied only up to 400 times in the life of an LPDDR2 device.

4.2.3.2 Power ON/OFF Sequences for Single Supply

Figure 4-9. ATSAMA5D27-WLSOM1 Single Supply Connection: Power-On Sequence

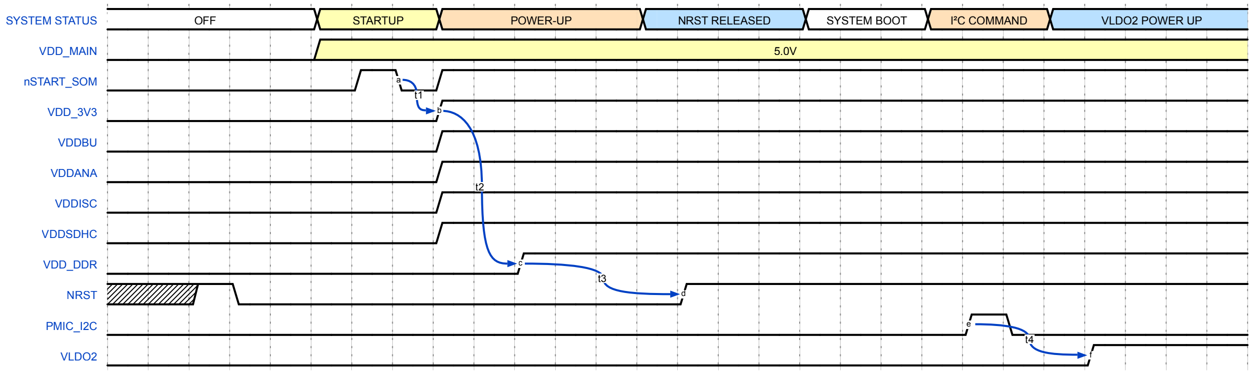


Figure 4-10. ATSAMA5D27-WLSOM1 Single Supply Connection: Power-Off Sequence

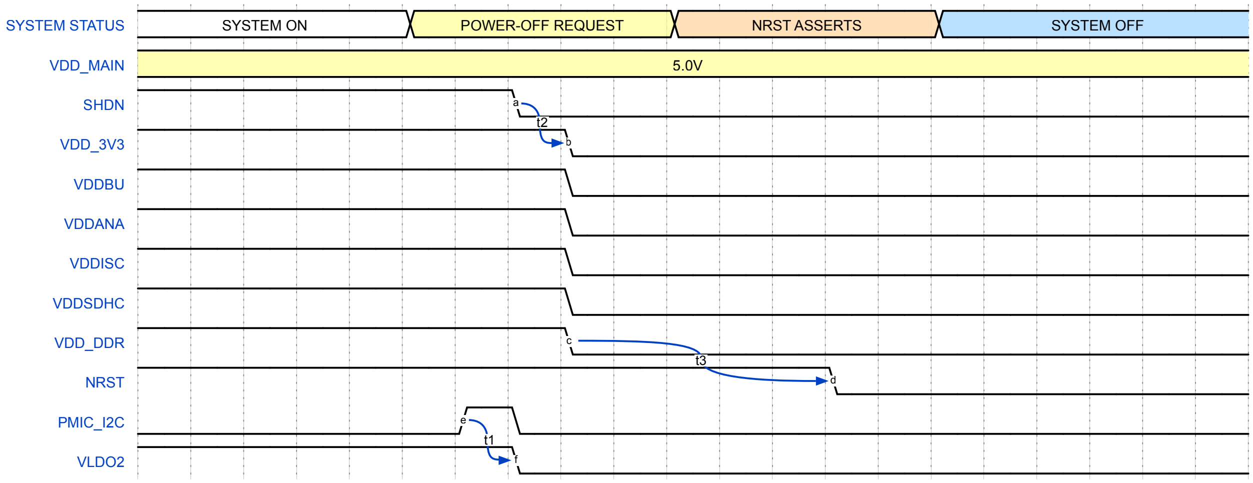


Table 4-1. ATSAMA5D27-WLSOM1 Simple Supply Timing Table

Symbol	Description	Min.	Typ.	Max.	Unit
t1	Power-Up Request Timing	0.5	–	2000	ms
t2	VDD_DDR Power-Up Timing	–	8	–	ms
t3	NRST Timing for Release	–	16	–	ms
t4	VLDO2 Power-Up Timing after I²C Request	–	0.5	1	ms
t5	VLDO2 Power-Down Timing after I²C Request	–	–	1	ms
t6	VDD_3V3 Power-Down Timing	–	10	–	µs
t7	NRST Forced to Low Timing	–	–	10	µs

4.2.3.3 Power ON/OFF Sequences for Multiple Supplies

Figure 4-11. ATSAMA5D27-WLSOM1 Multiple Supplies Connections: Power-On Sequence

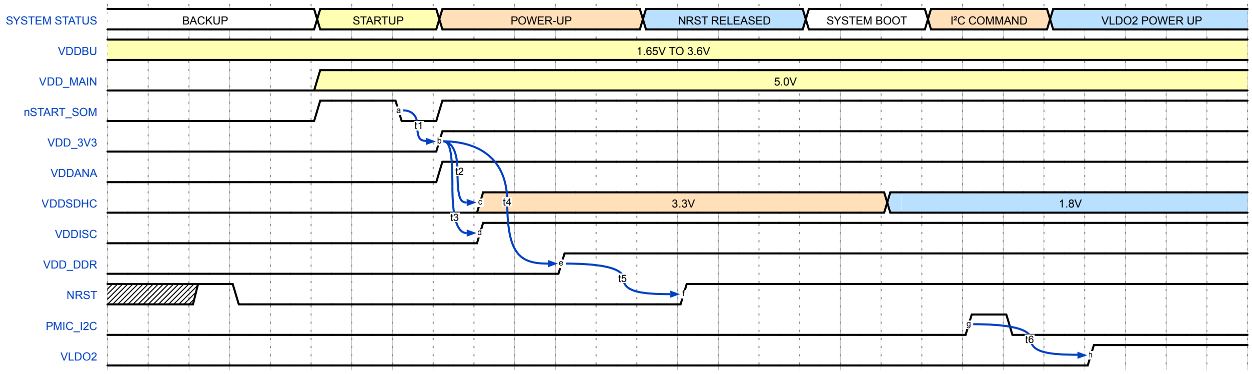


Figure 4-12. ATSAMA5D27-WLSOM1 Multiple Supplies Connections: Power-Off Sequence

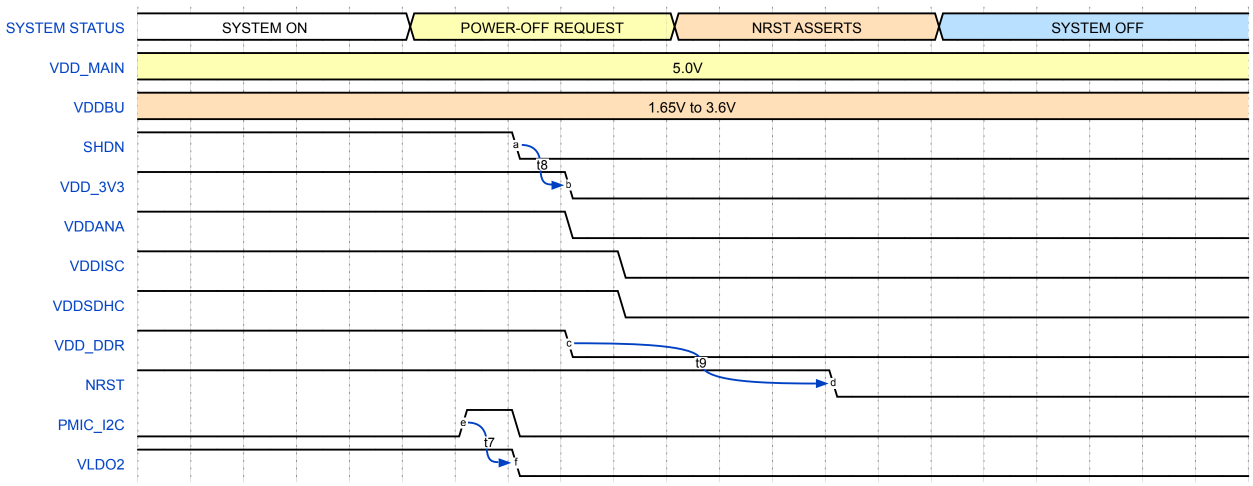


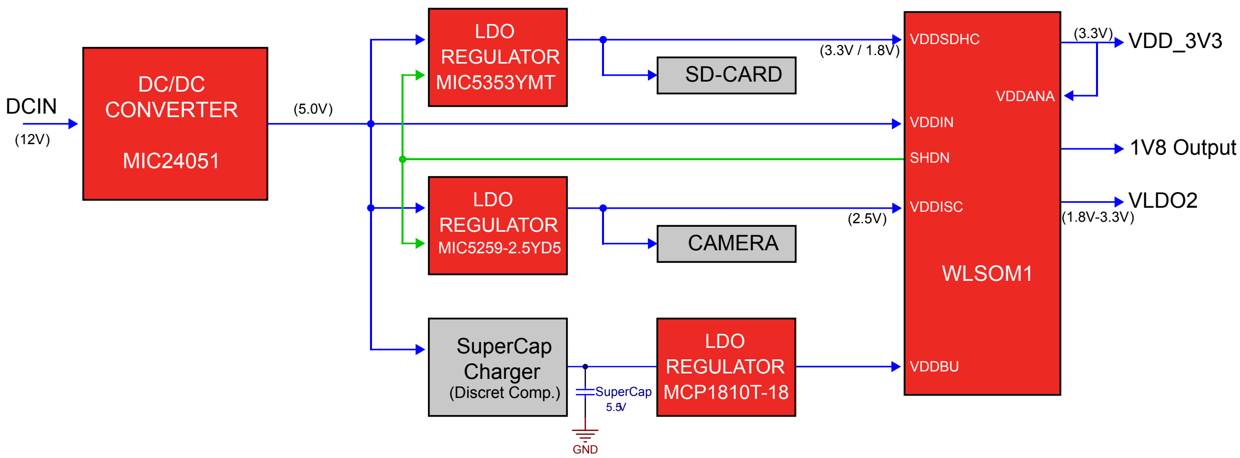
Table 4-2. ATSAMA5D27-WLSOM1 Multiple Supplies Timing Table

Symbol	Description	Min.	Typ.	Max.	Unit
t1	Power-Up Request Timing	0.5	–	2000	ms
t2	VDDSDHC Power-Up Timing	–	35	100	µs
t3	VDDISC Power-Up Timing	–	40	100	µs
t4	VDD_DDR Power-Up Timing	–	8	–	ms
t5	NRST Timing for Release	–	16	–	ms
t6	VLDO2 Power-Up Timing after I²C Request	–	0.5	1	ms
t7	VLDO2 Power-Down Timing after I²C Request	–	–	1	ms
t8	VDD_3V3 Power-Down Timing	–	10	–	µs
t9	NRST Forced to Low Timing	–	–	10	µs

4.2.4 Baseboard Power Delivery Application Diagram Example

The following figure is an example of power architecture at the baseboard level, input to the SOM and output from the SOM.

Figure 4-13. Baseboard Power Delivery Application Diagram Example



4.3 LAN Subsystem

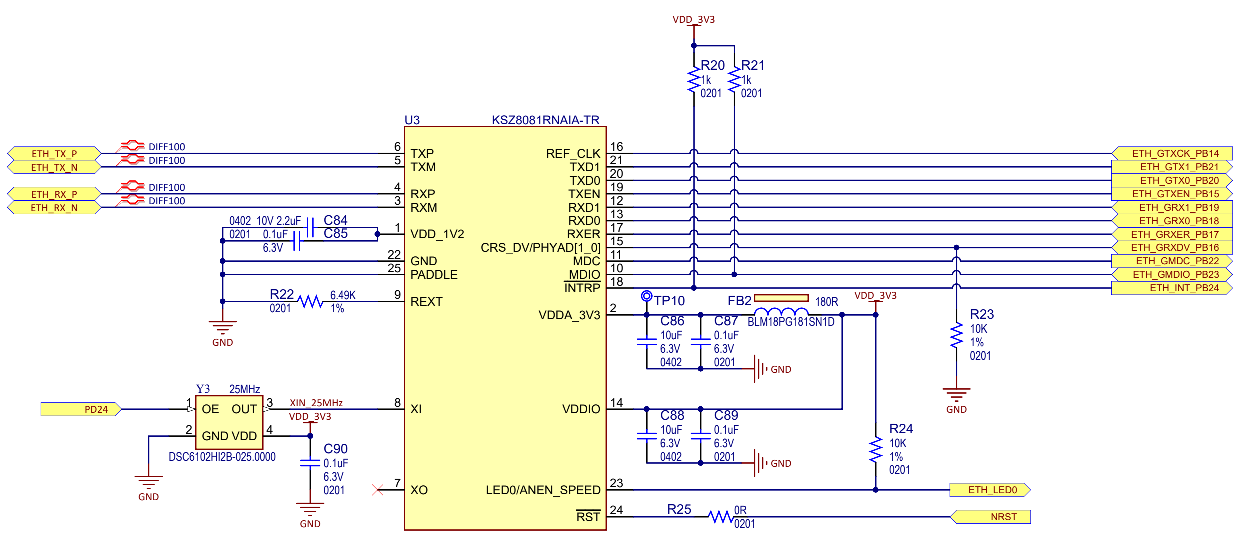
4.3.1 Ethernet Phy

The Microchip ATSAMA5D27-WLSOM1 embeds a single-supply 10Base-T/100Base-TX Ethernet physical layer transceiver for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors.

The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages. For more information, refer to the product web page.

Figure 4-14. Ethernet Phy Schematic



4.4 Voltage Threshold Detector

The Microchip ATSAMA5D27-WLSOM1 embeds a MIC842 micro-power, precision-voltage comparator with an on-chip voltage reference.

The device is intended for voltage monitoring applications. External resistors are used to set the voltage monitor threshold. When the threshold is crossed, the outputs switch polarity. Refer to the figures below.

The MIC842 incorporates a voltage reference and comparator with fixed internal hysteresis; two external resistors are used to set the switching threshold voltage.

Supply current is extremely low (1.5 µA, typical), making it ideal for portable applications.

The MIC842 is supplied in 4-pin 1.2 mm × 1.6 mm Thin DFN package. For more information, refer to the product web page.

Figure 4-15. Voltage Threshold Detector Schematic

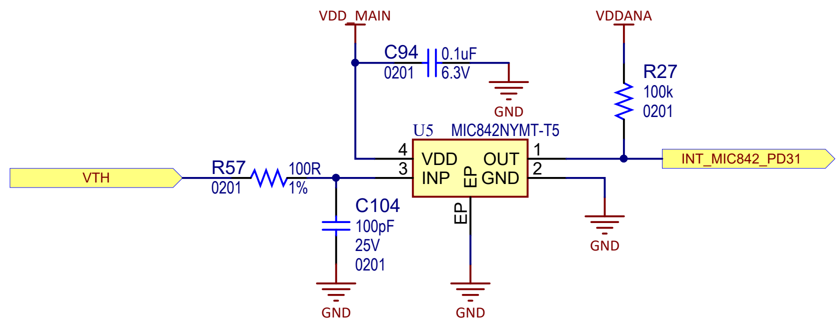


Figure 4-16. Voltage Threshold Detector Implementation Example

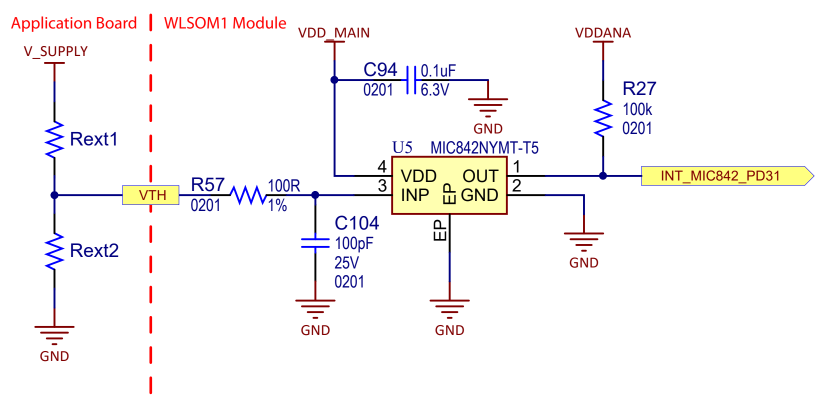


Table 4-3. Output Resistor Ladder Values and Input System Supply Example

System Supply Voltage	VTH Threshold Value	Rext1 Value	Rext2 Value
5V	4.64V	787 kΩ	287 kΩ
12V	11V	787 kΩ	100 kΩ
24V	21.78V	787 kΩ	47.5 kΩ
48V	39.51V	787 kΩ	25.5 kΩ

4.5 Radio Subsystem

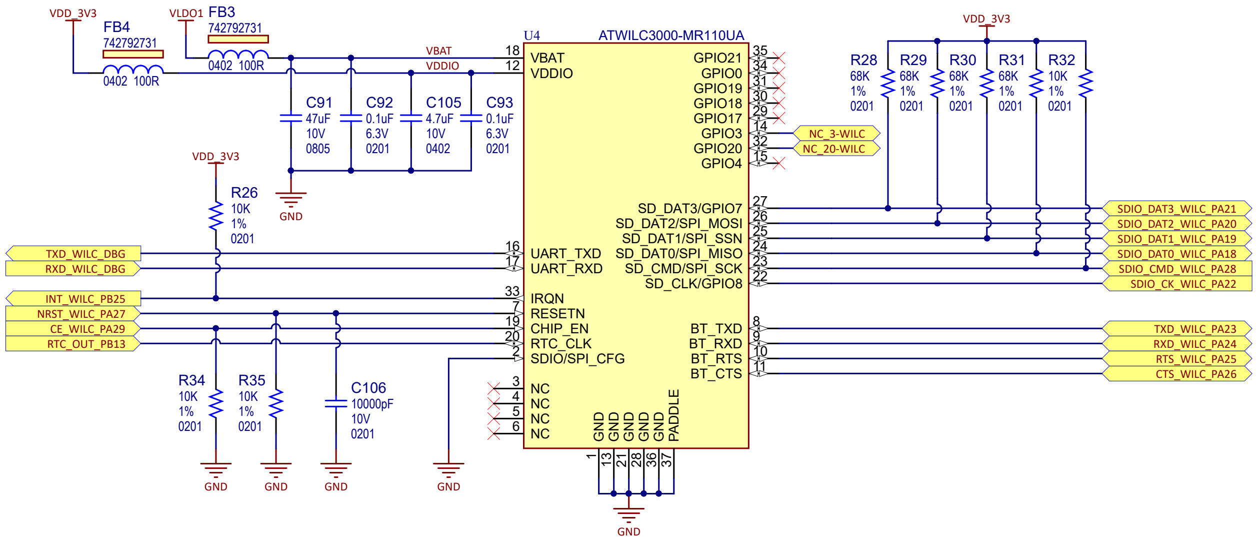
The ATSAMA5D27-WLSOM1 embeds an ATWILC3000, a single chip IEEE 802.11 b/g/n RF/Baseband/MAC link controller and Bluetooth 5. The ATWILC1000 connects to Microchip AVR®/SMART MCUs, SMART MPUs, and other processors with minimal resource requirements with simple SPI/SDIO-to-Wi-Fi and UART-to-Bluetooth interfaces.

The ATWILC3000 supports single stream 1x1 802.11n mode providing tested throughput of up to 46 Mbps UDP & 28 Mbps TCP/IP. The ATWILC3000 features fully integrated Power Amplifier, LNA, Switch and Power Management. Implemented in low-power CMOS technology, the ATWILC3000 offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC3000 utilizes highly optimized 802.11-Bluetooth coexistence protocols. The only external clock sources needed for the ATWILC3000 is a high-speed crystal or oscillator and a 32.768 kHz clock for sleep operation.

For more information, refer to the product web page.

Figure 4-17. Wi-Fi/BT Radio Subsystem Schematic



4.6 External Interfaces and PIO Muxing

4.6.1 PIO Muxing

Table 4-4. PIO Muxing: PIOA

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set
PA0	SDMMC0_CK	1	QSPI0_SCK	1	–	–	–	–	–	–	D0	2
PA1	SDMMC0_CMD	1	QSPI0_CS	1	–	–	–	–	–	–	D1	2
PA2	SDMMC0_DAT0	1	QSPI0_IO0	1	–	–	–	–	–	–	D2	2
PA3	SDMMC0_DAT1	1	QSPI0_IO1	1	–	–	–	–	–	–	D3	2
PA4	SDMMC0_DAT2	1	QSPI0_IO2	1	–	–	–	–	–	–	D4	2
PA5	SDMMC0_DAT3	1	QSPI0_IO3	1	–	–	–	–	–	–	D5	2
PA6	SDMMC0_DAT4	1	–	–	–	–	TIOA5	1	FLEXCOM2_IO0	1	D6	2
PA7	SDMMC0_DAT5	1	–	–	–	–	TIOB5	1	FLEXCOM2_IO1	1	D7	2
PA8	SDMMC0_DAT6	1	–	–	–	–	TCLK5	1	FLEXCOM2_IO2	1	NWE/NANDWE	2
PA9	SDMMC0_DAT7	1	–	–	–	–	TIOA4	1	FLEXCOM2_IO3	1	NCS3	2
PA10	SDMMC0_RSTN	1	–	–	–	–	TIOB4	1	FLEXCOM2_IO4	1	A21/NANDALE	2
PA11	SDMMC0_VDDSEL	1	–	–	–	–	TCLK4	1	–	–	A22/NANDCLE	2
PA12	SDMMC0_WP	1	IRQ	1	–	–	–	–	–	–	NRD/NANDOE	2
PA13	SDMMC0_CD	1	–	–	–	–	–	–	FLEXCOM3_IO1	1	–	–
PA14	SPI0_SPCK	1	TK1	1	–	–	I2SMCK1	2	FLEXCOM3_IO2	1	–	–
PA15	SPI0_MOSI	1	TF1	1	–	–	I2SCK1	2	FLEXCOM3_IO0	1	–	–

...........continued

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set
PA16	SPI0_MISO	1	TD1	1	–	–	I2SWS1	2	FLEXCOM3_IO3	1	–	–
PA17	SPI0_NPCS0	1	–	–	–	–	I2SDI1	2	FLEXCOM3_IO4	1	–	–
PA30	–	–	–	–	SPI0_NPCS0	2	PWMH0	1	–	–	–	–
PA31	–	–	–	–	SPI0_MISO	2	PWML0	1	–	–	–	–

Table 4-5. PIO Muxing: PIOB

PIO	A	IO set	C	IO set	D	IO set	F	IO set
PB00	–	–	SPI0_MOSI	2	PWMH1	1	–	–
PB01	–	–	SPI0_SPCK	2	PWML1	1	CLASSD_R0	1
PB02	–	–	–	–	PWMFI0	1	CLASSD_R1	1
PB03	URXD4	1	IRQ	3	PWMEXTRG0	1	CLASSD_R2	1
PB04	UTXD4	1	FIQ	4	–	–	CLASSD_R3	1
PB05	–	–	–	–	QSPI1_SCK	2	–	–
PB06	–	–	–	–	QSPI1_CS	2	–	–
PB07	–	–	–	–	QSPI1_IO0	2	–	–
PB08	–	–	–	–	QSPI1_IO1	2	–	–
PB09	–	–	–	–	QSPI1_IO2	2	–	–
PB10	–	–	–	–	QSPI1_IO3	2	–	–
PB11	–	–	URXD3	3	PDMIC_DAT0	2	–	–
PB12	–	–	UTXD3	3	PDMIC_CLK0	2	–	–
PB26	–	–	URXD0	1	PDMIC_DAT0	1	ISI_D0	3
PB27	–	–	UTXD0	1	PDMIC_CLK0	1	ISI_D1	3
PB28	–	–	FLEXCOM0_IO0	1	TIOA5	2	ISI_D2	3
PB29	–	–	FLEXCOM0_IO1	1	TIOB5	2	ISI_D3	3
PB30	–	–	FLEXCOM0_IO2	1	TCLK5	2	ISI_D4	3
PB31	–	–	FLEXCOM0_IO3	1	TWD0	1	ISI_D5	3

Table 4-6. PIO Muxing: PIOC

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set
PC00	–	–	–	–	FLEXCOM0_IO4	1	TWCK0	1	–	–	ISI_D6	3
PC01	–	–	–	–	CANTX0	1	SPI1_SPCK	1	I2SCK0	1	ISI_D7	3
PC02	–	–	–	–	CANRX0	1	SPI1_MOSI	1	I2SMCK0	1	ISI_D8	3
PC03	–	–	–	–	TIOA1	1	SPI1_MISO	1	I2SWS0	1	ISI_D9	3
PC04	–	–	–	–	TIOB1	1	SPI1_NPCS0	1	I2SDI0	1	ISI_PCK	3
PC05	–	–	–	–	TCLK1	1	SPI1_NPCS1	1	I2SDO0	1	ISI_VSYNC	3
PC06	–	–	–	–	–	–	SPI1_NPCS2	1	–	–	ISI_HSYNC	3
PC07	–	–	–	–	–	–	SPI1_NPCS3	1	–	–	ISI_MCK	3

...........continued

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set
PC09	FIQ	3	–	–	ISI_D0	1	TIOA4	2	–	–	–	–
PC10	LCDDAT2	2	–	–	ISI_D1	1	TIOB4	2	CANTX0	2	–	–
PC11	LCDDAT3	2	–	–	ISI_D2	1	TCLK4	2	CANRX0	2	A0/NBS0	2
PC12	LCDDAT4	2	–	–	ISI_D3	1	URXD3	1	TK0	2	A1	2
PC13	LCDDAT5	2	–	–	ISI_D4	1	UTXD3	1	TF0	2	A2	2
PC14	LCDDAT6	2	–	–	ISI_D5	1	–	–	TD0	2	A3	2
PC15	LCDDAT7	2	–	–	ISI_D6	1	–	–	RD0	2	A4	2
PC16	LCDDAT10	2	–	–	ISI_D7	1	–	–	RK0	2	A5	2
PC17	LCDDAT11	2	–	–	ISI_D8	1	–	–	RF0	2	A6	2
PC18	LCDDAT12	2	–	–	ISI_D9	1	–	–	FLEXCOM3_IO2	2	A7	2
PC19	LCDDAT13	2	–	–	ISI_D10	1	–	–	FLEXCOM3_IO1	2	A8	2
PC20	LCDDAT14	2	–	–	ISI_D11	1	–	–	FLEXCOM3_IO0	2	A9	2
PC21	LCDDAT15	2	–	–	ISI_PCK	1	–	–	FLEXCOM3_IO3	2	A10	2
PC22	LCDDAT18	2	–	–	ISI_VSYNC	1	–	–	FLEXCOM3_IO4	2	A11	2
PC23	LCDDAT19	2	–	–	ISI_HSYNC	1	–	–	–	–	A12	2
PC24	LCDDAT20	2	–	–	ISI_MCK	1	–	–	–	–	A13	2
PC25	LCDDAT21	2	–	–	ISI_FIELD	1	–	–	–	–	A14	2
PC26	LCDDAT22	2	–	–	–	–	CANTX1	1	–	–	A15	2
PC27	LCDDAT23	2	–	–	PCK1	2	CANRX1	1	–	–	A16	2
PC28	LCDPWM	2	FLEXCOM4_IO0	1	PCK2	1	–	–	–	–	A17	2
PC29	LCDDISP	2	FLEXCOM4_IO1	1	–	–	–	–	–	–	A18	2
PC30	LCDVSYNC	2	FLEXCOM4_IO2	1	–	–	–	–	–	–	A19	2
PC31	LCDHSYNC	2	FLEXCOM4_IO3	1	URXD3	2	–	–	–	–	A20	2

Table 4-7. PIO Muxing: PIOD

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set	Extra
PD0	LCDPCK	2	FLEXCOM4_IO4	1	UTXD3	2	GTSUCOMP	2	–	–	A23	2	–
PD1	LCDDEN	2	–	–	–	–	GRXCK	2	–	–	A24	2	–
PD2	URXD1	1	–	–	–	–	GTXER	2	ISI_MCK	2	A25	2	–
PD3	UTXD1	1	FIQ	2	–	–	GCRS	2	ISI_D11	2	NWAIT	2	PTC_ROW0
PD4	–	–	URXD2	1	–	–	GCOL	2	ISI_D10	2	NCS0	2	PTC_ROW1
PD5	–	–	UTXD2	1	–	–	GRX2	2	ISI_D9	2	NCS1	2	PTC_ROW2
PD6	TCK	2	PCK1	1	–	–	GRX3	2	ISI_D8	2	NCS2	2	PTC_ROW3
PD7	TDI	2	–	–	–	–	GTX2	2	ISI_D0	2	NWR1/NBS1	2	PTC_ROW4
PD8	TDO	2	–	–	–	–	GTX3	2	ISI_D1	2	NANDRDY	2	PTC_ROW5
PD9	TMS	2	–	–	–	–	GTXCK	2	ISI_D2	2	–	–	PTC_ROW6

...........continued

PIO	A	IO set	B	IO set	C	IO set	D	IO set	E	IO set	F	IO set	Extra
PD10	NTRST	2	–	–	–	–	GTXEN	2	ISI_D3	2	–	–	PTC_ROW7
PD11	TIOA1	3	PCK2	2	–	–	GRXDV	2	ISI_D4	2	–	–	PTC_COL0
PD12	TIOB1	3	FLEXCOM4_IO0	2	–	–	GRXER	2	ISI_D5	2	–	–	PTC_COL1
PD13	TCLK1	3	FLEXCOM4_IO1	2	–	–	GRX0	2	ISI_D6	2	–	–	PTC_COL2
PD14	TCK	1	FLEXCOM4_IO2	2	–	–	GRX1	2	ISI_D7	2	–	–	PTC_COL3
PD15	TDI	1	FLEXCOM4_IO3	2	–	–	GTX0	2	ISI_PCK	2	–	–	PTC_COL4
PD16	TDO	1	FLEXCOM4_IO4	2	–	–	GTX1	2	ISI_VSYNC	2	–	–	PTC_COL5
PD17	TMS	1	–	–	–	–	GMDC	2	ISI_HSYNC	2	–	–	PTC_COL6
PD18	NTRST	1	–	–	–	–	GMDIO	2	ISI_FIELD	2	–	–	PTC_COL7
PD19	–	–	TWD1	3	–	–	–	–	–	–	–	–	AD0
PD20	–	–	TWCK1	3	–	–	–	–	–	–	–	–	AD1
PD23	–	–	–	–	–	–	–	–	–	–	–	–	AD4
PD24	–	–	–	–	–	–	–	–	–	–	–	–	AD5
PD25	SPI1_SPCK	3	–	–	–	–	–	–	–	–	–	–	AD6
PD26	SPI1_MOSI	3	–	–	FLEXCOM2_IO0	2	–	–	–	–	–	–	AD7
PD27	SPI1_MISO	3	TCK	3	FLEXCOM2_IO1	2	–	–	–	–	–	–	AD8
PD28	SPI1_NPCS0	3	TDI	3	FLEXCOM2_IO2	2	–	–	–	–	–	–	AD9
PD29	SPI1_NPCS1	3	TDO	3	FLEXCOM2_IO3	2	TIOA3	3	–	–	–	–	AD10
PD30	SPI1_NPCS2	3	TMS	3	FLEXCOM2_IO4	2	TIOB3	3	–	–	–	–	AD11

4.6.2 Interfacing with an SD Card

The SD (Secure Digital) Card is a non-volatile memory card format used as mass storage memory in mobile devices.

Secure Digital Multimedia Card (SDMMC) Controller

The ATSAMA5D27-WLSOM1 has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

The SDMMC0 interface can be connected to a standard SD card interface.

SDMMC0 Card Connector

The board features a standard MMC/SD card connector, connected to SDMMC0. The SDMMC0 communication is based on a 4- or 8-pin interface (clock, command, four or eight data and power lines). It may include a card detection switch.

The figures below illustrate the implementation for the SDMMC0 interface for a 4-bit interface and for an 8-bit interface with a power switch for the supply of the digital interface for high-speed interface management.

Figure 4-18. 4-/8-bit SD-Card Power Switch Example Schematic

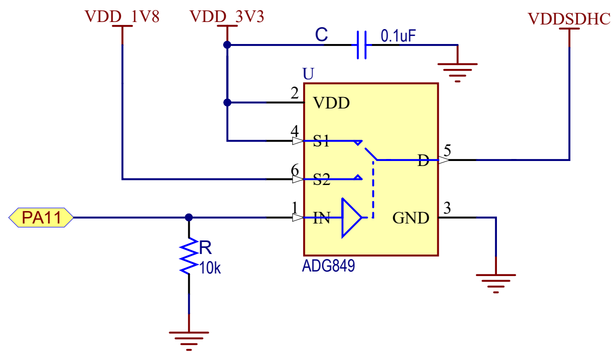


Figure 4-19. 4-bit SD-Card Interface Example Schematic

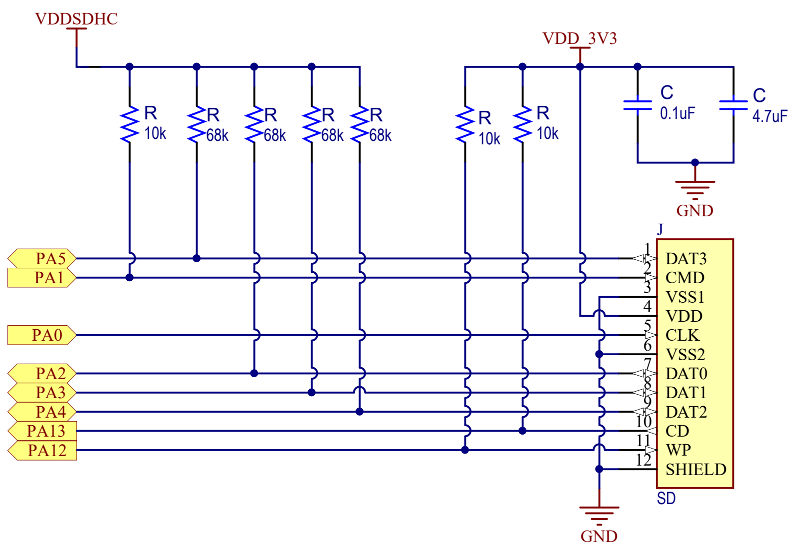
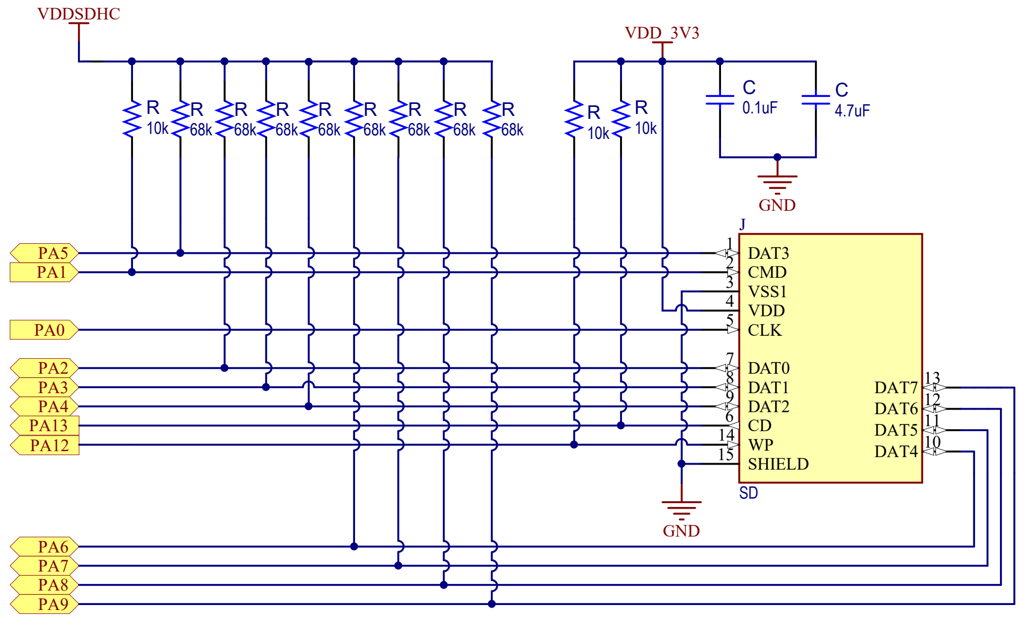


Figure 4-20. 8-bit SD-Card Interface Example Schematic



4.6.3 Interfacing with e-MMC

The Secure Digital Multimedia Card (SDMMC) Controller supports the Embedded MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

In the example below, one MTFC4GLDEA 4 GB eMMC is connected to the processor through the SDMMC0 port.

Table 4-8. SDMMC Reference Documents

Name	Link
SD Host Controller Simplified Specification V3.00	www.sdcard.org
SDIO Simplified Specification V3.00	www.sdcard.org
Physical Layer Simplified Specification V3.01	www.sdcard.org
Embedded MultiMedia Card (e.MMC) Electrical Standard 4.51	www.jedec.org

Figure 4-21. e-MMC Power Switch Example Schematic

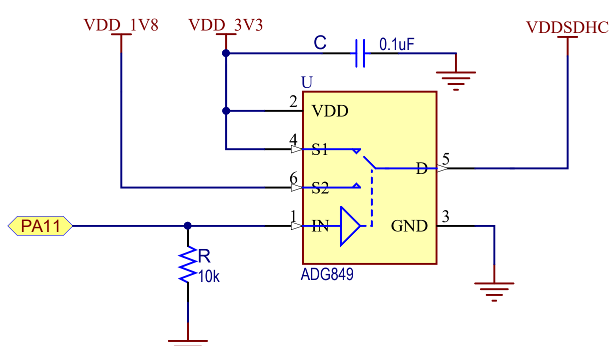
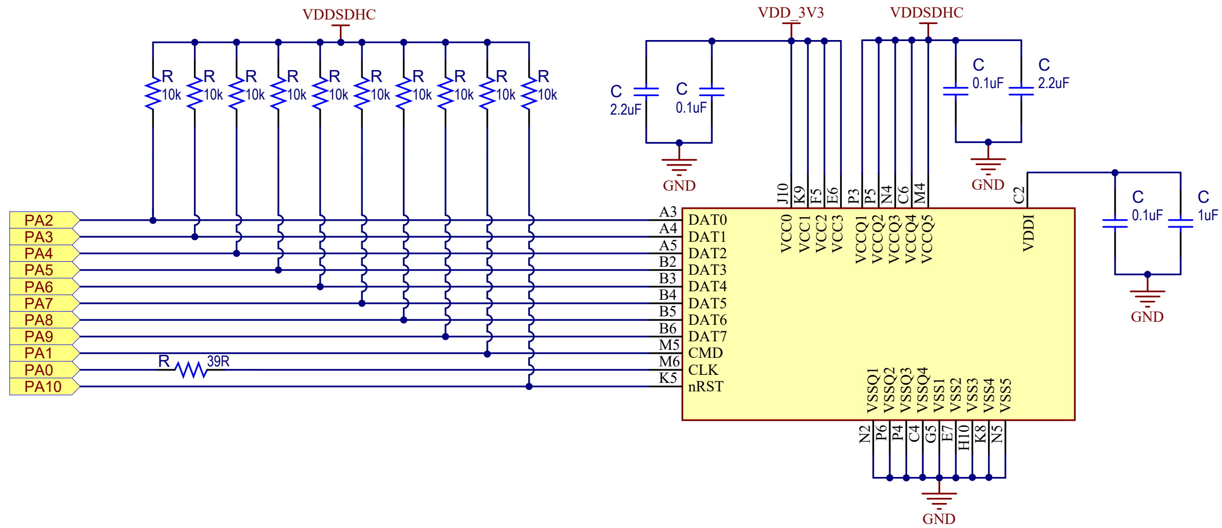


Figure 4-22. e-MMC Interface Example Schematic



4.6.4 Interfacing with NAND Flash

This Static Memory Controller (SMC) is capable of handling several types of external memory and peripheral devices, such as SRAM, PSRAM, PROM, EPROM, EEPROM, LCD module, NOR Flash and NAND Flash.

The SMC generates the signals that control the access to external memory devices or peripheral devices.

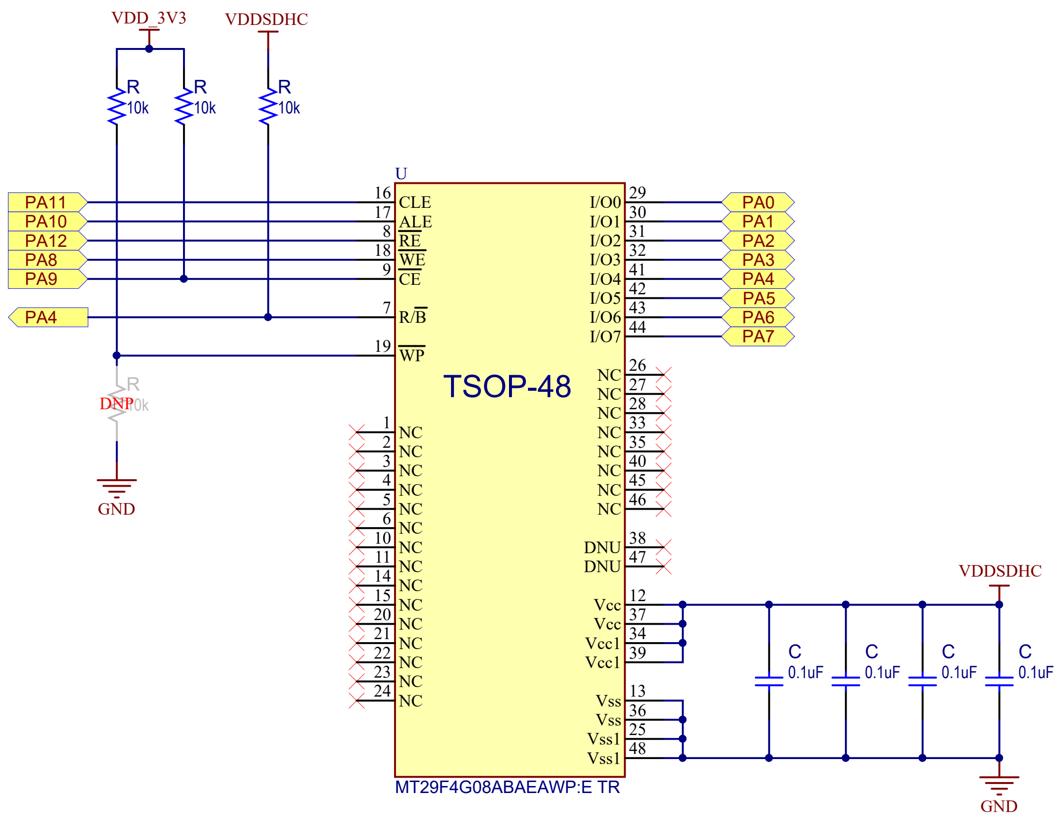
The SMC embeds a NAND Flash Controller (NFC). The NFC can handle automatic transfers, sending the commands and address cycles to the NAND Flash and transferring the contents of the page (for read and write) to the NFC SRAM. It minimizes the CPU overhead.

The SMC includes programmable hardware error correcting code with one-bit error correction capability and supports two-bit error detection.

In order to improve the overall system performance, the DATA phase of the transfer can be DMA-assisted.

An example below is given with 8-bit NAND Flash memory from Micron.

Figure 4-23. NAND Flash Interface Example Schematic



4.6.5 Interfacing with a Camera

The Image Sensor Controller (ISC) system manages incoming data from a parallel sensor. It supports a single active interface. The parallel interface protocol can use a free-running clock or a gated clock strategy. It supports the ITU-R BT 656/1120 422 protocol with a data width of 8 bits or 10 bits and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion and horizontal and vertical chrominance subsampling module. The module also integrates a triple channel Direct Memory Access Controller master interface.

Two different schematics examples are shown below with different Image Sensor supply voltages.

Figure 4-24. Camera Interface Example Schematic with VDDISC Set at 3.3V

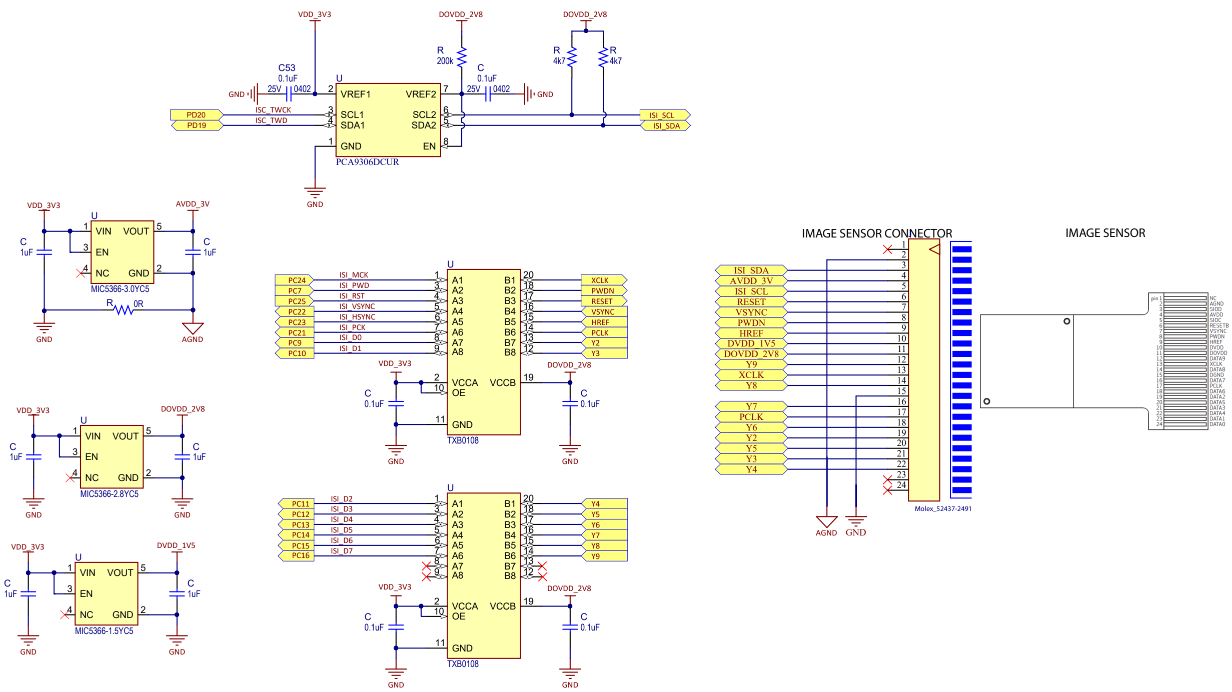
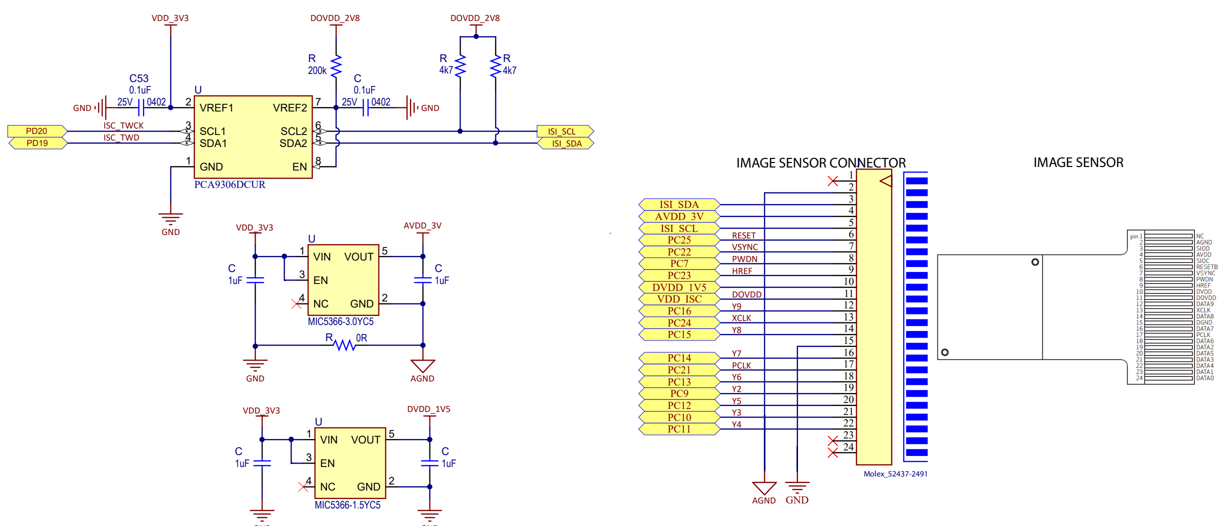


Figure 4-25. Camera Interface Example Schematic with VDDISC Set at Specific Voltage



4.6.6 Connecting to the SPI Interface

Four different FLEXCOM interfaces, with seven possible configurations (configured in SPI mode), and two pure SPI Interfaces, with four possible configurations, are available on the ATSAMA5D27-WLSOM1 module.

The Flexible Serial Communication Controller (FLEXCOM) offers several serial communication protocols that are managed by the three submodules USART, SPI, and TWI.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the “master”' which controls the data flow, while the other devices act as “slaves'' which have data shifted into and out by the master. Different CPUs can take turn being masters (multiple master protocol, contrary to single master protocol where one CPU is always the master while all of the others are always slaves). One master can simultaneously shift data into multiple slaves. However, only one slave can drive its output to write data back to the master at any given time.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS).

The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI)—This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO)—This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the master and regulates the flow of the data bits. The master can transmit data at a variety of baud rates; there is one SPCK pulse for each bit that is transmitted.
- Slave Select (NSS)—This control line allows slaves to be turned on and off by hardware.

Table 4-9. SPI Interface Configurations

Interface Instance	IO set	Pin #	PIO	Pin Name	Comments
SPI0	1	21	PA14	SPI0_SPCK	
SPI0	1	22	PA15	SPI0_MOSI	
SPI0	1	23	PA16	SPI0_MISO	
SPI0	1	24	PA17	SPI0_NPCS0	
SPI0	2	76	PA30	SPI0_NPCS0	
SPI0	2	75	PA31	SPI0_MISO	
SPI0	2	81	PB00	SPI0_MOSI	
SPI0	2	80	PB01	SPI0_SPCK	
SPI0	1	18	PC01	SPI1_SPCK	
SPI1	1	17	PC02	SPI1_MOSI	
SPI1	1	16	PC03	SPI1_MISO	
SPI1	1	19	PC04	SPI1_NPCS0	
SPI1	1	20	PC05	SPI1_NPCS1	
SPI1	1	176	PC06	SPI1_NPCS2	
SPI1	1	177	PC07	SPI1_NPCS3	
SPI1	3	132	PD25	SPI1_SPCK	
SPI1	3	127	PD26	SPI1_MOSI	
SPI1	3	123	PD27	SPI1_MISO	
SPI1	3	124	PD28	SPI1_NPCS0	
SPI1	3	131	PD29	SPI1_NPCS1	
SPI1	3	130	PD30	SPI1_NPCS2	

Table 4-10. FLEXCOM Interfaces Configurations in SPI Mode

Interface Instance	IO set	Pin #	PIO	Pin Name	Comments
FLEXCOM0	1	28	PB28	FLEXCOM0_IO0	MOSI Signal
FLEXCOM0	1	27	PB29	FLEXCOM0_IO1	MISO Signal
FLEXCOM0	1	30	PB30	FLEXCOM0_IO2	SPCK Signal
FLEXCOM0	1	26	PB31	FLEXCOM0_IO3	NPCS0 Signal
FLEXCOM0	1	15	PC00	FLEXCOM0_IO4	NPCS1 Signal
FLEXCOM2	1	171	PA06	FLEXCOM2_IO0	MOSI Signal
FLEXCOM2	1	173	PA07	FLEXCOM2_IO1	MISO Signal
FLEXCOM2	1	167	PA08	FLEXCOM2_IO2	SPCK Signal
FLEXCOM2	1	172	PA09	FLEXCOM2_IO3	NPCS0 Signal
FLEXCOM2	1	168	PA10	FLEXCOM2_IO4	NPCS1 Signal
FLEXCOM2	2	127	PD26	FLEXCOM2_IO0	MOSI Signal
FLEXCOM2	2	123	PD27	FLEXCOM2_IO1	MISO Signal
FLEXCOM2	2	124	PD28	FLEXCOM2_IO2	SPCK Signal
FLEXCOM2	2	131	PD29	FLEXCOM2_IO3	NPCS0 Signal
FLEXCOM2	2	130	PD30	FLEXCOM2_IO4	NPCS1 Signal
FLEXCOM3	2	56	PC18	FLEXCOM3_IO2	SPCK Signal
FLEXCOM3	2	70	PC19	FLEXCOM3_IO1	MISO Signal
FLEXCOM3	2	58	PC20	FLEXCOM3_IO0	MOSI Signal
FLEXCOM3	2	63	PC21	FLEXCOM3_IO3	NPCS0 Signal
FLEXCOM3	2	65	PC22	FLEXCOM3_IO4	NPCS1 Signal
FLEXCOM4	1	39	PC28	FLEXCOM4_IO0	MOSI Signal
FLEXCOM4	1	38	PC29	FLEXCOM4_IO1	MISO Signal
FLEXCOM4	1	34	PC30	FLEXCOM4_IO2	SPCK Signal
FLEXCOM4	1	36	PC31	FLEXCOM4_IO3	NPCS0 Signal
FLEXCOM4	1	33	PD00	FLEXCOM4_IO4	NPCS1 Signal
FLEXCOM4	2	119	PD12	FLEXCOM4_IO0	MOSI Signal
FLEXCOM4	2	116	PD13	FLEXCOM4_IO1	MISO Signal
FLEXCOM4	2	117	PD14	FLEXCOM4_IO2	SPCK Signal
FLEXCOM4	2	114	PD15	FLEXCOM4_IO3	NPCS0 Signal
FLEXCOM4	2	115	PD16	FLEXCOM4_IO4	NPCS1 Signal

4.6.7 Connecting to the I²C Interface

Four different FLEXCOM interfaces, with seven possible configurations (configured in TWI mode), and one pure TWI Interface are available on the ATSAMA5D27-WLSOM1 module.

The Flexible Serial Communication Controller (FLEXCOM) offers several serial communication protocols that are managed by the three submodules USART, SPI, and TWI.

The Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 kbit/s in Fast mode and up to 3.4 Mbit/s in High-Speed Slave mode only, based on a byte-oriented transfer format.

It can be used with any Two-wire Interface bus Serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), Dot Matrix/Graphic LCD Controller and temperature sensor. The TWI is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported.

Table 4-11. I²C Interface Configurations

Interface Instance	IO set	Pin #	PIO	Pin Name	Comment
TWI1	3	120	PD19	TWD1	No need of external pull-up. Already integrated in ATSAMA5D27-WLSOM1 module
TWI1	3	122	PD20	TWCK1	
FLEXCOM0	1	28	PB28	FLEXCOM0_IO0	Need external pull-up in case of FLEXCOM interface use as I²C/TWI interface.
FLEXCOM0	1	27	PB29	FLEXCOM0_IO1	
FLEXCOM2	1	171	PA6	FLEXCOM2_IO0	
FLEXCOM2	1	173	PA7	FLEXCOM2_IO1	
FLEXCOM2	2	127	PD26	FLEXCOM2_IO0	
FLEXCOM2	2	123	PD27	FLEXCOM2_IO1	
FLEXCOM3	1	22	PA15	FLEXCOM3_IO0	
FLEXCOM3	1	175	PA13	FLEXCOM3_IO1	
FLEXCOM3	2	58	PC20	FLEXCOM3_IO0	
FLEXCOM3	2	63	PC21	FLEXCOM3_IO1	
FLEXCOM4	1	39	PC28	FLEXCOM4_IO0	
FLEXCOM4	1	38	PC29	FLEXCOM4_IO1	
FLEXCOM4	2	119	PD12	FLEXCOM4_IO0	
FLEXCOM4	2	116	PD13	FLEXCOM4_IO1	

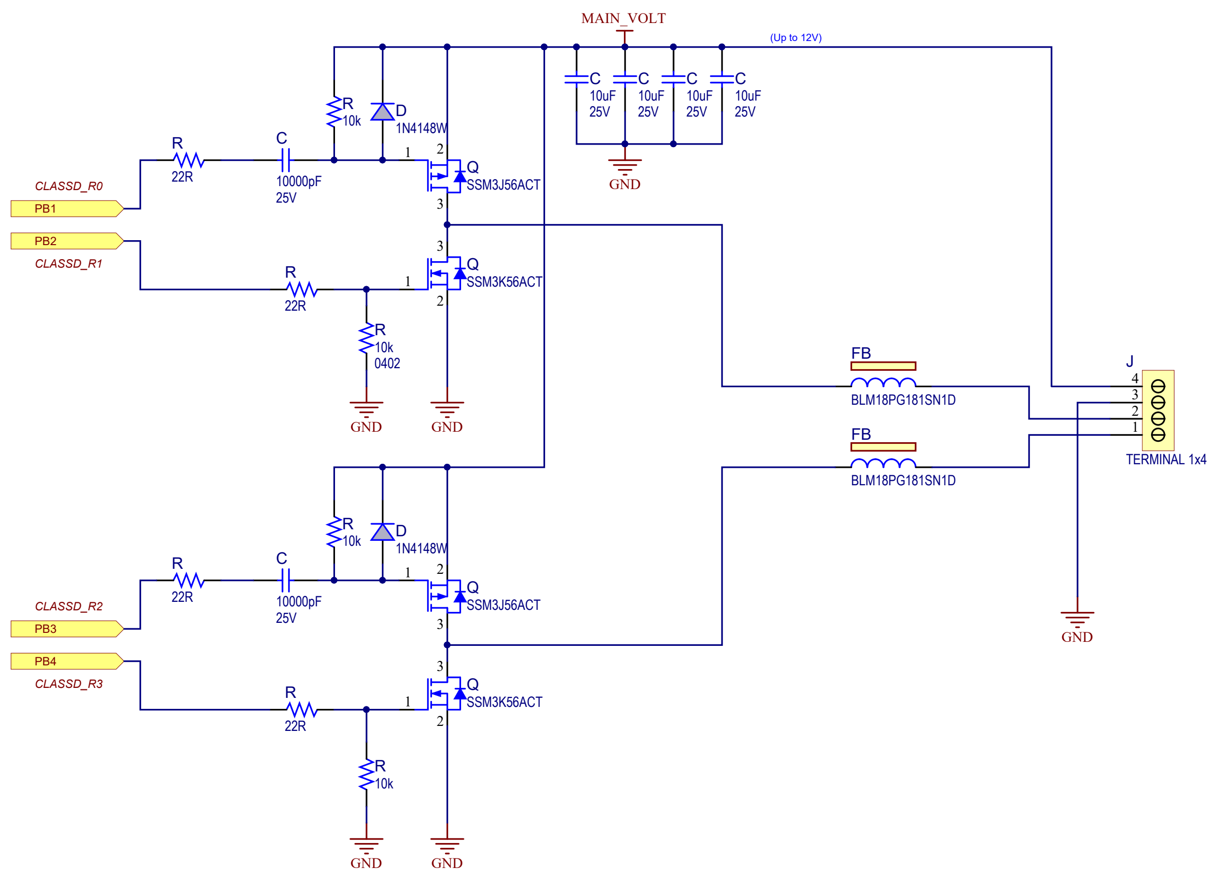
4.6.8 Interfacing with CLASS-D Audio Output

The Audio Class D Amplifier (CLASSD) is a digital input, pulse width modulated (PWM) output mono Class D amplifier. It features a high-quality interpolation filter embedding a digitally controlled gain, an equalizer and a de-emphasis filter.

On its input side, the CLASSD is compatible with most common audio data rates. On the output side, its PWM output can drive either:

- high-impedance single-ended or differential output loads (Audio DAC application) or,
- external MOSFETs through an integrated non-overlapping circuit (Class D power amplifier application).

Figure 4-26. CLASS-D Interface Example Schematic



4.7 Antenna

4.7.1 Certified Antenna References

The ATSAMA5D27-WLSOM1 is FCC-ID certified with the following antenna references. In case of use of another reference, the end customer must pass another full certification.

Table 4-12. ATSAMA5D27-WLSOM1 Certified Antenna References

P/N	Vendor	Antenna Gain @ 2.4 GHz Band	Antenna Type	Cable Length/ Remarks
RFA-02-P33	Aristotle	2 dBi	PCB	150 mm
RFA-02-D3	Aristotle	2dBi	Dipole	150 mm
RFA-02-G03	Aristotle	2dBi	Metal Stamp	150 mm
RFA-02-L2H1	Aristotle	2 dBi	Dipole	150 mm
RFA-02-P05	Aristotle	2 dBi	PCB	150 mm
RFA-02-C2M2	Aristotle	2 dBi	Dipole	SMA to u.FL cable length of 100 mm

4.7.2 Antenna Placement Recommendations

Particular attention must be given to the placement of the antenna and its cable. The following recommendations must be applied:

- Ensure that the antenna cable is not expected to be routed over circuits generating electrical noise on the Host board.
- Antenna on the module should not be placed in direct contact or in close proximity of the plastic casing/objects.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise, signals or harmonics within the 2.4 GHz to 2.5 GHz frequency band away from the antenna and, if possible, shield those components. Any noise radiated from the host board in this frequency band degrades the sensitivity of the module.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
I/O Supply Voltage	VDDANA, VDDISC, VDDSDHC	-0.3	4.0	V
Fuse Supply Voltage	VDDFUSE	-0.3	3.0	V
Main Supply Voltage	VDD_MAIN	-0.3	6.0	V
Backup Supply Voltage	VDDBU	-0.3	4.0	V
Storage Temperature	$T_{STORAGE}$	-55	150	°C
RF Input Power Maximum	–	–	23	dBm
Maximum Input Current	VDD_MAIN	–	2	A

5.2 Recommended Operating Conditions

The following table provides the operating ratings for the ATSAMA5D27-WLSOM1 module.

Table 5-2. Recommended Operating Ratings

Characteristic	Symbol	Min.	Max.	Unit
I/O Supply Voltage	VDDANA, VDDISC, VDDSDHC	1.6	3.6	V
Fuse Supply Voltage	VDDFUSE	2.25	2.75	V
Main Supply Voltage	VDD_MAIN	3.0	5.5	V
Backup Supply Voltage	VDDBU	1.65	3.6	V
Operating Temperature	T_A	-40	85	°C

5.3 DC Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 5-3. DC Electrical Characteristics for GPIO Inputs

Pad	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	All GPIO @ 3.3V	-0.3	–	0.4	V
V_{IH}	High-level Input Voltage	All GPIO @ 3.3V	2.3	–	3.6	V
V_{OL}	Low-level Output Voltage	I0 Max.	–	–	0.41	V
V_{OH}	High-level Output Voltage	I0 Max.	2.9	–	–	V

...........continued

Pad	Parameters	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low-level Input Current	All GPIO @ 3.3V	-1	–	1	µA
I_{IH}	High-level Input Current	All GPIO @ 3.3V	-1	–	1	µA
I_{OL}	Low-level Output Current	All GPIO @ 3.3V / Low	-2	–	–	mA
		All GPIO @ 3.3V / High	-32	–	–	mA
I_{OH}	High-level Output Current	All GPIO @ 3.3V / Low	–	–	2	mA
		All GPIO @ 3.3V / High	–	–	32	mA

5.4 Radio Performances

Refer to the ATWILC3000 data sheet, section 4.4, “IEEE 802.11 b/g/n Radio Performance”.

Refer to the ATWILC3000 data sheet, section 4.5, “Bluetooth Radio Performance”.

6. Mechanical Characteristics

6.1 Module Outline Drawings

Figure 6-1. ATSAMA5D27-WLSOM1 Module Drawing

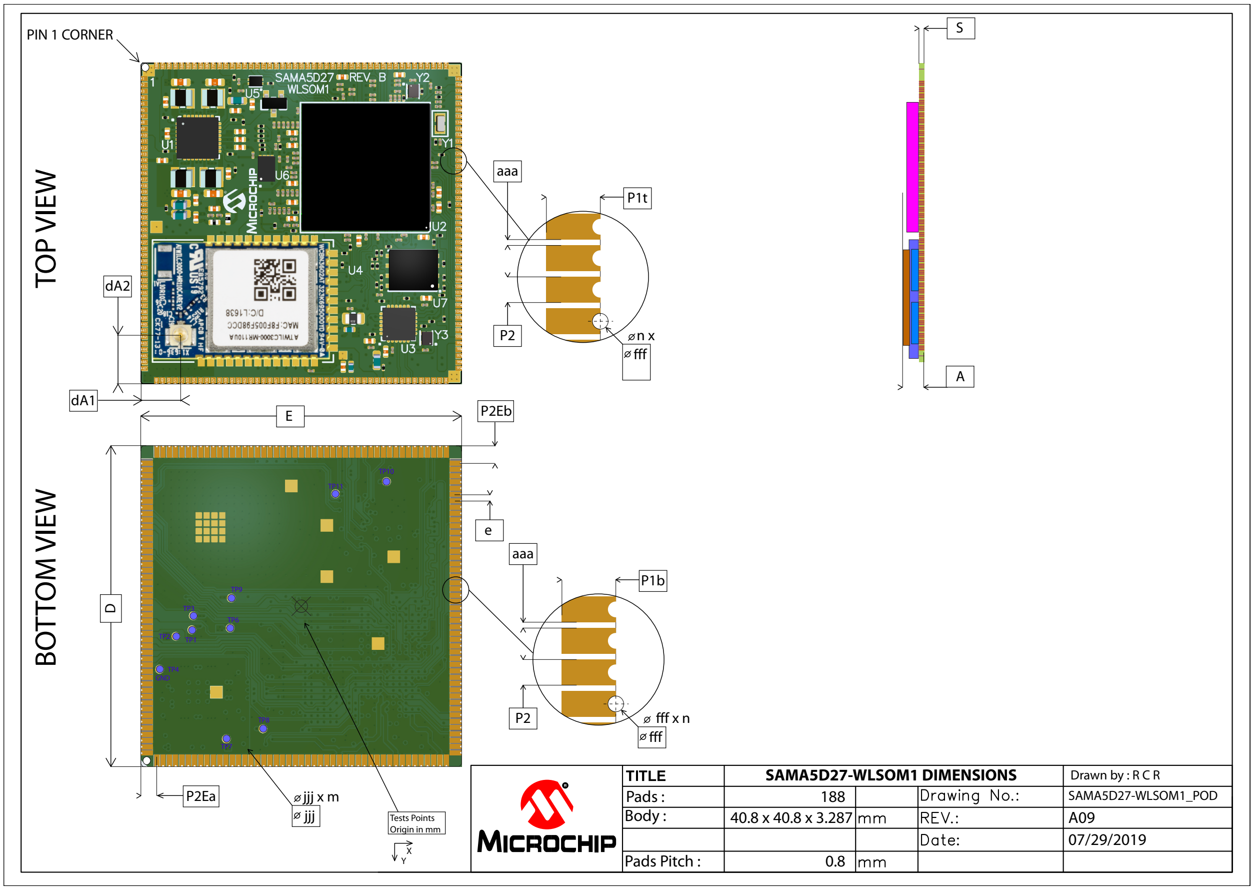


Table 6-1. ATSAMA5D27-WLSOM1 Module Dimensions (in mm)

		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
Body Size	X	E	40.700	40.800	40.900	
	Y	D	40.700	40.800	40.900	
Pad Pitch		E	–	0.800	–	
PCB Thickness		S	1.150	1.200	1.250	
Total Thickness		A1	–	3.287	3.387	
Pad Length (1)	Top Side	P1t	–	0.800	–	
	Bottom Side	P1b	–	1.500	–	
Pad Width (1)		P2	–	0.600	–	Solder Mask Defined 0.550
Pad Space (1)		aaa	–	0.200	–	

...........continued						
		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
Opening Drill Diameter		fff	–	0.400	–	
Pad Count		n	–	188	–	
Test Point Diameter		jjj	–	1.000	–	
Test Point Count		m	–	10	–	
Pad Axis to Edge [(1)]	X	P2Ea	–	2.000	–	
	Y	P2Eb	–	2.000	–	
U.FL Antenna Axis to Edge	X	dA1	–	5.011	–	
	Y	dA2	–	6.161	–	

Note:

1. Tolerances are defined upon:
   – IPC A600 – Class2
   – IPC 2615
2. Test points placed under module are for production purposes only. No connection on these points is allowed. They are listed to avoid any contact with the main board vias or copper areas.

Table 6-2. Test Point Position Compared to Center Origin

Test Point Number	X	Y	Voltage Point
TP1	-13.875	3.000	VDDUTMII
TP2	-15.900	3.825	VDD_3V3
TP3	-13.700	1.225	VDDOSC_PLL
TP4	-17.975	8.000	GND
TP6	-9.025	2.775	VDDIODDR
TP7	-9.500	16.825	VDDCORE
TP8	-4.850	15.550	VDDPLAA
TP9	-8.875	-1.025	VLDO1
TP10	10.825	-15.800	VDDA_3V3
TP11	4.350	-14.250	VBAT

6.2 Module Land Pattern (Host Board PCB Footprint)

Figure 6-2. ATSAMA5D27-WLSOM1 Land Pattern Drawing

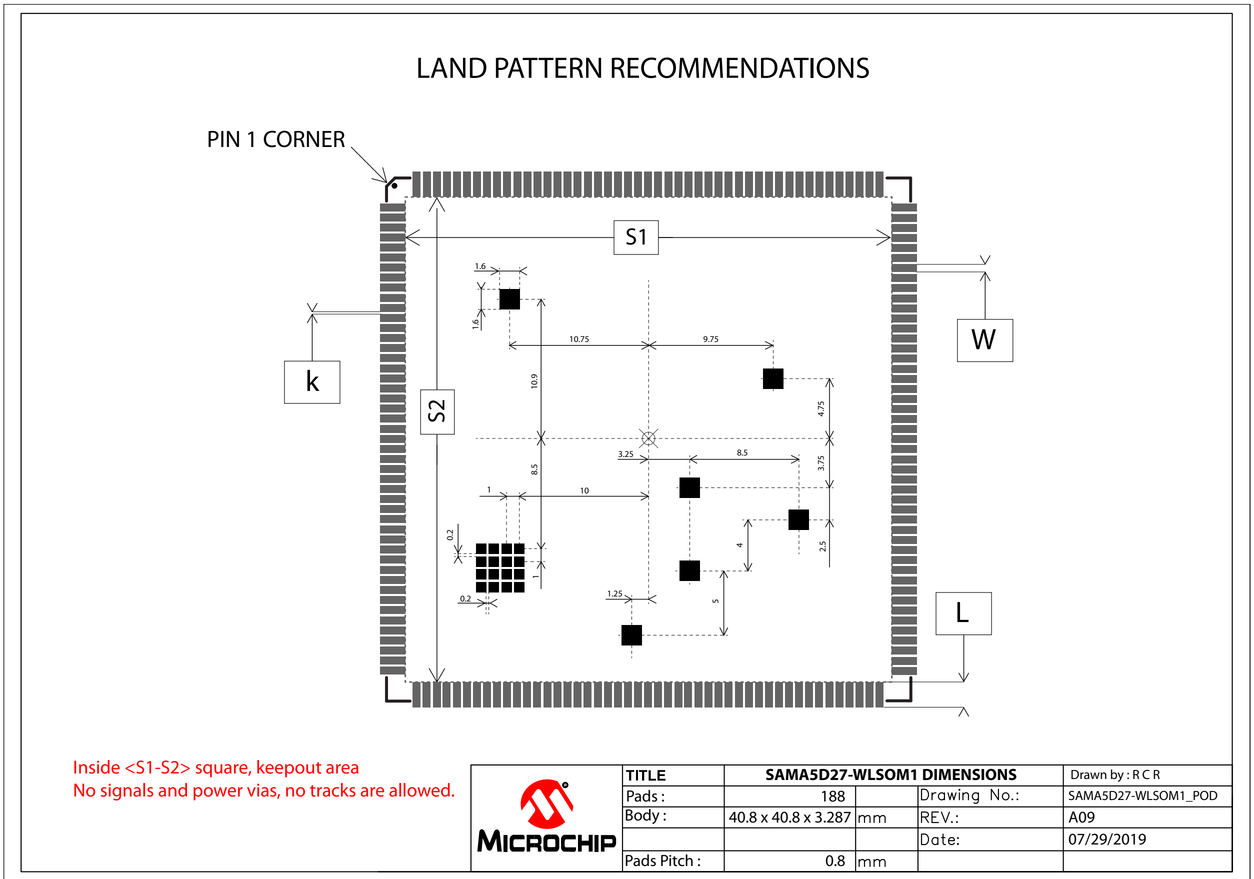
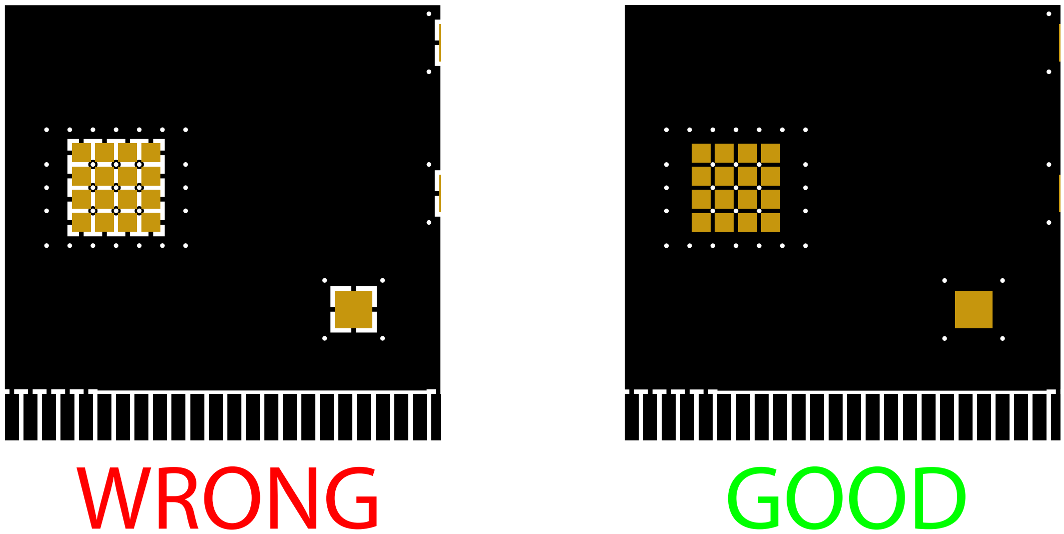


Table 6-3. ATSAMA5D27-WLSOM1 Land Pattern Dimensions (in mm)

	Symbol	Common Dimensions			Comments
		Min.	Typ.	Max.	
Land Pattern Pad Width	W	–	0.600	–	Solder Mask Defined 0.550
Land Pattern Pad Length	L	–	2.000	–	
Land Pattern Pad X Space	S1	–	37.800	–	
Land Pattern Pad Y Space	S2	–	37.800	–	
Land Pattern Pad Space	k	–	0.200	–	

Figure 6-3. GND Pads Overview and Layout Recommendation



Note: It is recommended to use the layout as shown on the right above. This solution increases RF performance of the Wi-Fi and Bluetooth communications and optimizes heat sink capability of the system; on the host board, do not apply thermal brakes on the TOP layout around GND pads.

6.3 Other Characteristics

Table 6-4. ATSAMA5D27-WLSOM1 Other Characteristics

Parameter	Measurement		Comments
	Value	Unit	
Weight	7.91	g	

7. Assembly and Storage Information

7.1 Storage Condition

7.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored at a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product is 12 months from the date the bag is sealed.

7.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, RH < 30%.

7.2 Motherboard Solder Paste

The SnAgCu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, or SENJU M705-GRN360-K-V, no clean paste.

7.3 Motherboard Stencil Design

The recommended stencil is a laser-cut, stainless-steel type with thickness of 100 µm to 130 µm and an approximate ratio of 1:1 for stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25 µm larger than the top is utilized. Local manufacturers may find other combinations of stencil thickness and aperture size to get good results.

7.4 Bake Information

The ATSAMA5D27-WLSOM1 module is rated MSL 3, indicating that storage and assembly processes must be compliant with IPC/JEDEC J-STD-033C.

The ATSAMA5D27-WLSOM1 module has a total thickness of 3.287 mm (PCB and SMD mounted) and is comparable to a die package. Thus baking instructions must comply with Table 4-1 of J-STD-033-C as a package body comprised between 2.0 mm and 4.5 mm.

Refer to the highlighted information in the table below.

Figure 7-1. IPC/JEDEC Table

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days
Thickness >1.4 mm ≤2.0 mm	2	18 hours	15 hours	63 hours	2 days	25days	20 days
	2a	21 hours	16 hours	3 days	2 days	29 days	22 days
	3	27 hours	17 hours	4 days	2 days	37 days	23 days
	4	34 hours	20 hours	5 days	3 days	47 days	28 days
	5	40 hours	25 hours	6 days	4 days	57 days	35 days
	5a	48 hours	40 hours	8 days	6 days	79 days	56 days
Thickness >2.0 mm ≤4.5 mm	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days
BGA package >17 mm x 17 mm or any stacked die package (See Note 2)	2-6	96 hours	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level

7.5 Reflow Profile

The ATSAMA5D27-WLSOM1 is assembled using standard lead-free reflow profile IPC/JEDEC J-STD-020E.

In addition to the initial assembly solder, we recommend a maximum of two additional soldering processes:

- the assembly on main board
- a spare heating pass in case the module must be removed from the main board for analysis

The ATSAMA5D27-WLSOM1 can be soldered to the host PCB by using the standard and lead-free solder reflow profile. To avoid damage to the module, follow the JEDEC recommendations as well as those listed below:

- Do not exceed the peak temperature (Tp) of 245ºC.
- Refer to the solder paste data sheet for specific reflow profile recommendations.
- Use no-clean flux solder paste.
- Use only one flow. If the PCB requires multiple flows, mount the module at the time of the final flow.

Figure 7-2. Reflow Profile Example used for Soldering ATSAMA5D27-WLSOM1 Module on ATSAMA5D27-WLSOM1-EK1 Board

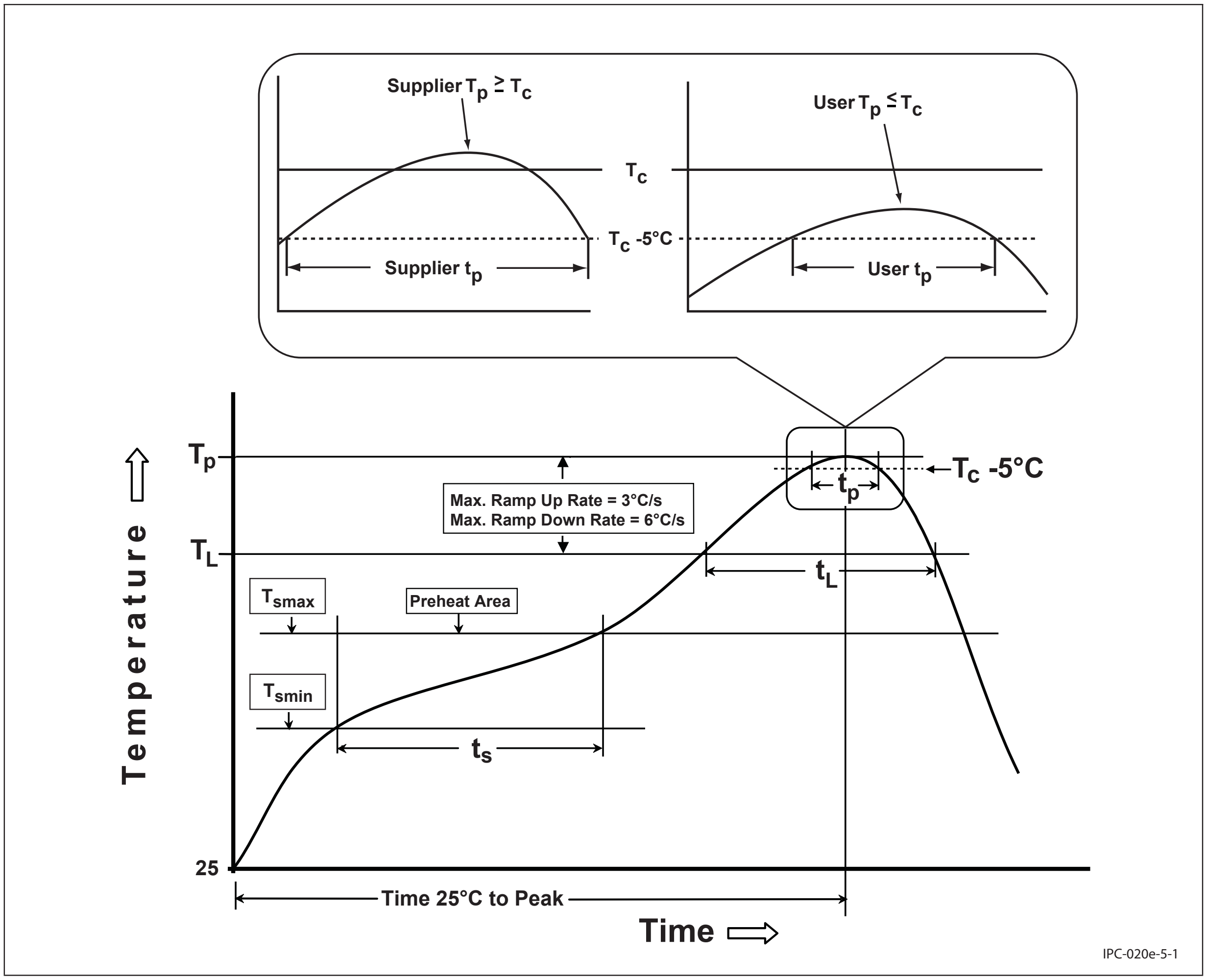


Table 7-1. Reflow Profile Table Parameters

Profile Feature		J-STD-020E Profile
Pre-heat Temperature Min	T_{smin}	150°C
Pre-heat Temperature Max	T_{smax}	200°C
Temperature Rise	ts (from T_{smin} to T_{smax})	60 to 120 seconds
Ramp-up Rate	T_L to T_p	3°C/sec. max.
Liquidous Temperature Time maintained above 217°C	t_L	60 to 150 seconds
Peak Temperature	T_P	245°C
Time (t_P) within 5°C of the specified classification temperature (T_C)	t_P	30 seconds
Ramp-down rate	T_P to T_L	6°C/sec. max.
Time 25°C to peak temperature	–	8 minutes max.

8. Regulatory Approval

Refer to the ATWILC3000 data sheet, section 16.

9. Ordering Information

Table 9-1. Ordering Details

Ordering Code	Package	Description	Regulatory Information
ATSAMA5D27-WLSOM1	40.8 x 40.8 x 3.287 mm	Certified Microchip MPU Wireless module with SAMA5D27, WILC3000 and U.FL connector	FCC, IC, CE

10. Revision History

10.1 Rev. A - 10/2019

First issue.

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ATSAMA5 D27 - WLSOM1

Architecture

Product Group

Architecture:	ATSAMA5	= Arm Cortex-A5 CPU
Product Group:	D27-WLSOM1	Certified MPU Wireless module with SAMA5D27, WILC3000 and U.FL connector

Examples:

- ATSAMA5D27-WLSOM1 = System-On-Module (SOM) based on the SAMA5D27, with 2 Gb LPDDR2 SDRAM running up to 500 MHz, and a Wi-Fi/BT Wireless module

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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